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SERVICE MANUAL

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Technical Information

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

VIDEO CASSETTE RECORDER

January 1987 **TOKAI WORKS**

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1. P IN P (DIGITAL MEMORY) CIRCUIT

1-1. OUTLINE (See Fig. 1-1.)

This P IN P (Picture in Picture) function creates a sub-screen by reducing the main screen (E-E picture) or other source screen (only during playback) to approx. 1/9 in the ratio of area at one of the 4 corners of the main screen.

The figure at the top left shows the original picture with one-field component consisting of the effective screen section (within broken lines) and non-effective screen section of the retrace line period. The vertical axis shows the number of horizontal scanning lines (H) and the horizontal axis shows the number (C: Column) obtained by dividing the horizontal scanning period using the 3fc clock pulse (three times the color subcarrier frequency) to explain the principles of sub-screen video processing.

The sampling area of the original picture required to compose the sub-screen is determined from 36H to 228H for the vertical axis and from 34C to 682C for the horizontal axis as shown by the solid lines in the figure. The upper and lower areas outside the effective screen (between 14.5H and 36H and between 228H and 259H) are not sampled due to the limitation of the memory. The information in the retrace line period from horizontal 32C to 96C is used for playback of DC components of color-difference signals to reproduce the tone of the sub-screen correctly.

To reduce the area of the original picture to approx. 1/9, two among three scanning lines and columns are suppressed for both the horizontal and vertical directions and the remaining lines and columns are derived and A/D (Analog/Digital) converted and are then stored temporarily in the DRAM (Dynamic Random Access Memory: called the P IN P memory hereafter) for the composition of the sub-screen and time axis conversion. By suppressing two among three scanning lines and columns, a sub-screen consisting of 64H scanning lines x 216C columns is composed in the P IN P memory. The tone (amplitude: set to maximum 1Vp-p) is quantized to 6 bits. The P IN P memory must have a memory capacity of 331776 bits (64 vertical x 216 horizontal x 6 quantization x 4 fields) to store 4-field components of digital sub-screen data (64H x 216C) quantized to 6 bits. One of the 4 field memories is used for writing and one of the other 3 memories is selected and read matching the interlace scanning of the main screen.

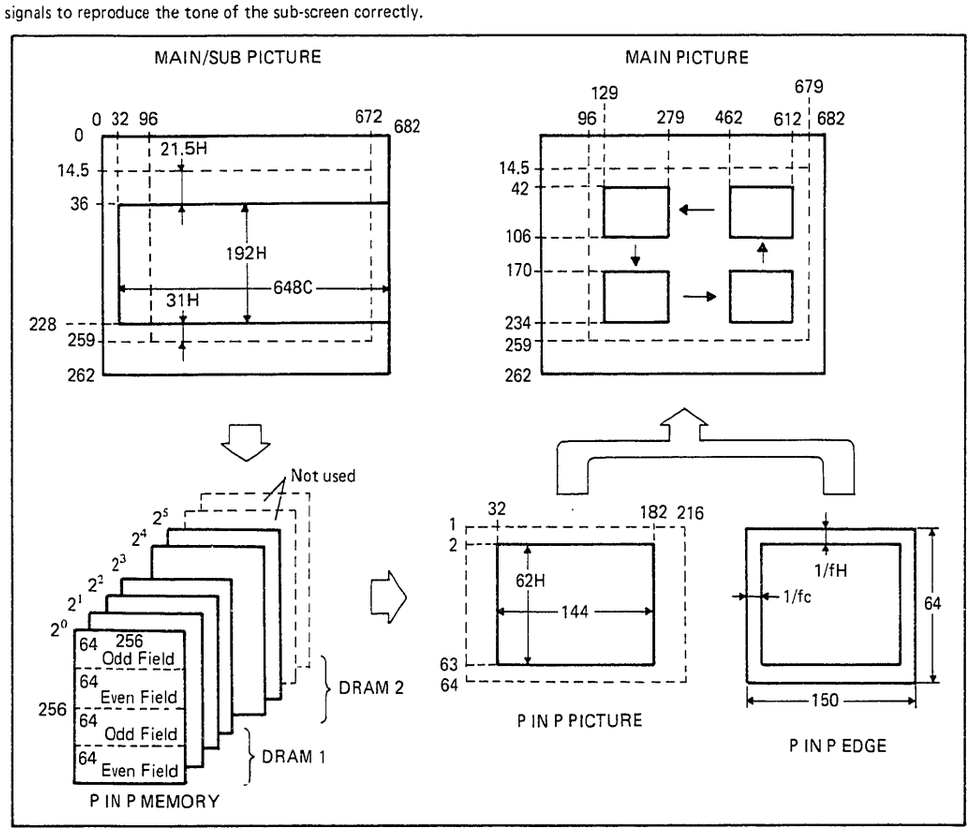


Fig. 1-1 Sub-screen Video Processing Principle

The P IN P memory in this unit uses 2 ICs each of which incorporates 4 pairs of memory cell arrays with the memory capacities of 65536 bits (256 rows x 256 columns), and utilizing 6 pairs, allocates them to each bit for 6-bit quantization. With each pair of memory cell arrays, vertical addresses 256 are divided by four to ensure a sub-screen writing area of 4 field components (64 vertical x 256 horizontal x 4 fields).

Since the sub-screen data must be written to the memory in real time, and simultaneously, the previously written sub-screen data must be read out, each of the 6 pairs of memory cell arrays is driven in parallel so the write and read modes are the same, and a line memory buffer of 1 row x 256 columns exclusively used for the read-out and a 6-bit write standby memory buffer are provided. Writing to the memory cell array is performed at the speed of fc, the data transfer from the memory cell array to the line memory buffer is at fH and the reading from the line memory buffer is at 3fc. The writing standby memory buffer is used to hold the data to be written temporarily when data is transferred from the memory cell array to the line memory buffer.

With the digital sub-screen data stored in the P IN P memory, the field picture data matching the interlace scanning of the main screen is selected and synchronized with the scanning of the main screen and is then read out at the speed of 3fc. The data is D/A converted and synchronized with fc of the main screen and finally replaces the video signal at one of the 4 corners of the main screen. The 62H x 144C area of the sub-screen data consisting of 64H x 216C is displayed on the main screen and the other scanning lines and columns are used for the following 2 purposes. Some of the scanning lines and columns are overlapped over the main screen section so the video signal is not missing when scanning is switched from the main screen to the sub-screen and vice versa. The other scanning lines/columns align the pedestal levels of the demodulated color-difference signals to match the tints of both the main and sub-screens.

The sub-screen is edged in white to emphasize the border between the sub-screen and main screen. The edge line is determined at 1/fH vertical x 1/fc horizontal. During edging, a DC voltage equivalent to 100% white level is superimposed on the video signal on the edge portions. The position of the edge sub-screen framed in the main screen can be selected by the remote control unit to one of the 4 corners of the effective screen as shown at the top right in the figure.

The above is an overview of sampling of the sub-screen and framing it in the main screen. The following describes the processing of the video signal for the sub-screen.

1-2. Sub-screen Video Signal Processing Principle (See Fig. 1-2.)

The video signal of the original picture is separated into its luminance signal (Y) and two color-difference signals (R-Y, B-Y) and is demodulated and sampled. This is because, since two among three scanning lines and columns are suppressed, the original picture is reduced to 1/9 (area ratio) and the sub-screen is formed, the correct phase data of the burst signal and chroma signals cannot be obtained without the above operations and the correct tint is not determined.

The sampling frequencies are approx. 2.4 MHz (4fc/6) and 0.6 MHz (fc/6) for the Y signal and R-Y/B-Y signals. Since the maximum frequencies of each signal must be half of the sampling frequencies, the frequency bands of the separated and demodulated Y, R-Y and B-Y signals are limited by the lowpass filters. The band-limited Y, R-Y and B-Y signals are time-divided by the multiplexer in the following order at the speed of fc and are applied to the A/D converter.

Since the sampling frequency of the color-difference signals is determined to be approx. 1/4 the frequency of the Y signal and the memory capacity must be saved, the multiplexer selects the Y signal 4 times and R-Y and B-Y signals once respectively to time-divide them when sampling the signals 6 times.

The digital Y, R-Y and B-Y signals read from the P IN P memory are processed in the reverse way to writing through the demultiplexer, D/A converter, LPF and the NTSC modulator, and a video signal for the sub-screen whose size is converted is formed.

Since the sub-screen must be framed in the specified position on the main screen correctly and the same tint must be obtained when the EE video signal is selected on both the main and sub-screens, the sync signal and burst signal in the main-screen video signal are used for the timing of reading from the P IN P memory and the producing of a chroma subcarrier signal necessary for NTSC modulation.

1-3. Circuit Configuration (See Fig. 1-3.)

The P IN P (Digital Memory) circuit is between the video output circuit and luma/chroma circuit, the same as the OSD circuit in a VTR with an OSD (On-Screen Display) function. The P IN P (Digital Memory) circuit is on the digital process circuit board. Since the digital process circuit board handles pulse signals with a maximum frequency of 10.74 MHz (3fc), it is housed in a shield case so it does not interfere with other circuits.

The P IN P circuit block consists of the following 14 circuits.

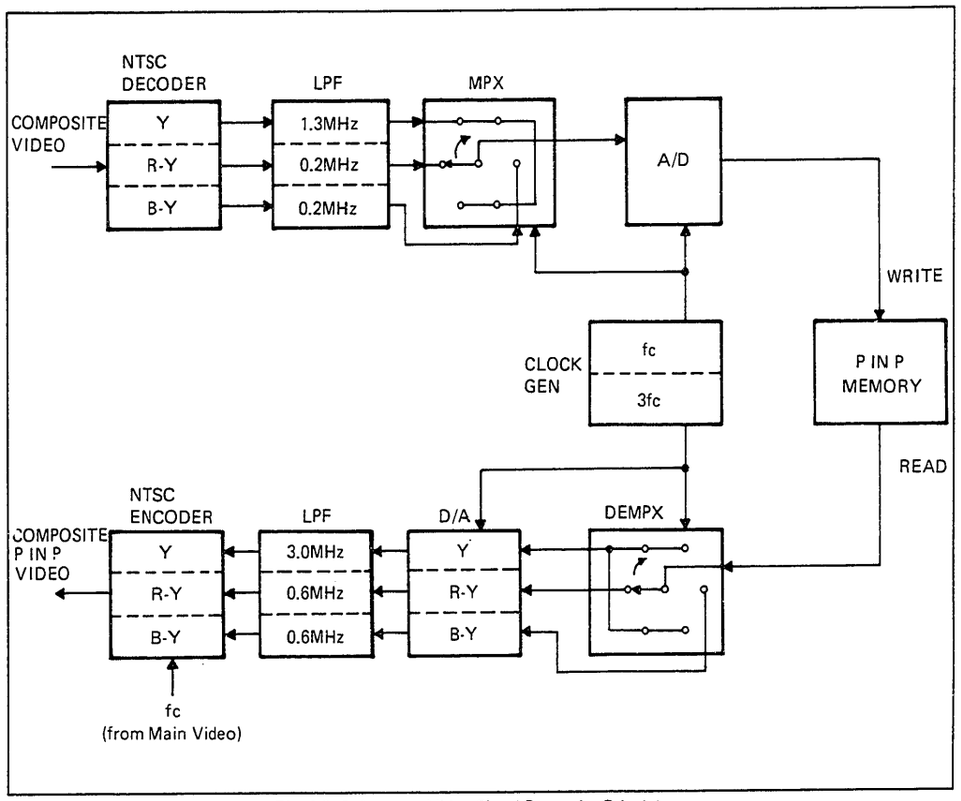


Fig. 1-2 Sub-screen Video Signal Processing Principle

– P IN P Controller (IC1002) –

This receives the three control signals (P IN P, P IN P INV, P IN P POSITION) from the system control μP and controls the overall P IN P circuit as follows.

- Sets the VTR to the P IN P mode.
- Selects the video signals of the main and sub-screens in the P IN P mode.
- Determines the position into which the sub-screen is framed.
- Generates a multiplexer control signal.
- Determines the clamp timing of the color-difference signals.
- Outputs a clock signal for A/D conversion of the sub-screen.
- Determines the operation period of the NTSC demodulator.
- Inputs the sync signals separated from the video signals of both the main and sub-screens and generates control signals for writing and reading to/from the P IN P memory.
- Converts the digital sub-screen video signal read from the P IN P memory in parallel to a luminance signal (Y) and color-difference signals (R-Y, B-Y) using the internal demultiplexer and supplies them to the D/A converter.

– P IN P Memory (IC1010, IC1011) –

These 2 ICs have the memory capacity of 524288 bits and store 4 field picture components of the digital sub-screen video signal quantized to 6 bits. The writing and reading of data are apparently performed in real time.

– Clock Signal Generator (IC1025) –

Generates a 3-phase clock signal equivalent to 3fc synchronized with the video signals of both the main and sub-screens necessary for the write and read operations of the P IN P memory.

– A/D Converter (IC1012) –

Converts the sub-screen video signal with the maximum value of 1 Vp-p separated into the Y, R-Y and B-Y signals and demodulated to a digital signal quantized to 6 bits. The clock signal necessary for A/D conversion is obtained from the P IN P controller.

– Clamper/Multiplexer (IC1024) –

The clamper sets the amplitudes of the R-Y and B-Y signals within the maximum amplitude of the Y signal before A/D conversion and then the multiplexer divides three signals at the speed of fc to convert them to serial signals. The clamp timing signal of the clamper and the time division control signal of the multiplexer are output from the P IN P controller.

– NTSC Demodulator/LPF (IC1023) –

The NTSC demodulator separates the sub-screen video signal into the luminance and color-difference signals to demodulate it and then the lowpass filter (LPF) limits the maximum frequency of the signal to be processed to half the sampling frequency.

– Main/Sub Video Input Switch (IC1202) –

Selects the video signal supplied to the main and sub-screen video processing circuits. This select command is output from the P IN P controller.

– D/A Converter/LPF (IC1022) –

The D/A converter converts the digital Y, R-Y and B-Y signals quantized to 6 bits to analog signals and then the lowpass filter (LPF) shapes the waveform and limits it within the NTSC specified frequency band.

– Clamper/NTSC Modulator (IC1021) –

The clamper aligns the color-difference signals, R-Y and B-Y, before being converted to chroma signals and then the NTSC modulator modulates the signal to an NTSC video signal using fc with the same phase as the main screen burst signal. The clmap timing signal is output from the P IN P controller.

– Main Screen Video Processor (IC1201, IC1205) –

Performs the following 2 controls for the main screen video signal.

- ACC controls the video signal from the built-in tuner or video input jack to keep the amplitude of the chroma carrier signal constant.
- Applies the chroma subcarrier signal to the NTSC modulator to modulate the color-difference signals to an NTSC signal.

– P IN P Switch/P IN P Edge Switch (IC1203) –

Replaces the video signal the position of which is determined by the P IN P controller with the sub-screen video signal and edge signal. This output is applied to the RF modulator and video output jack.

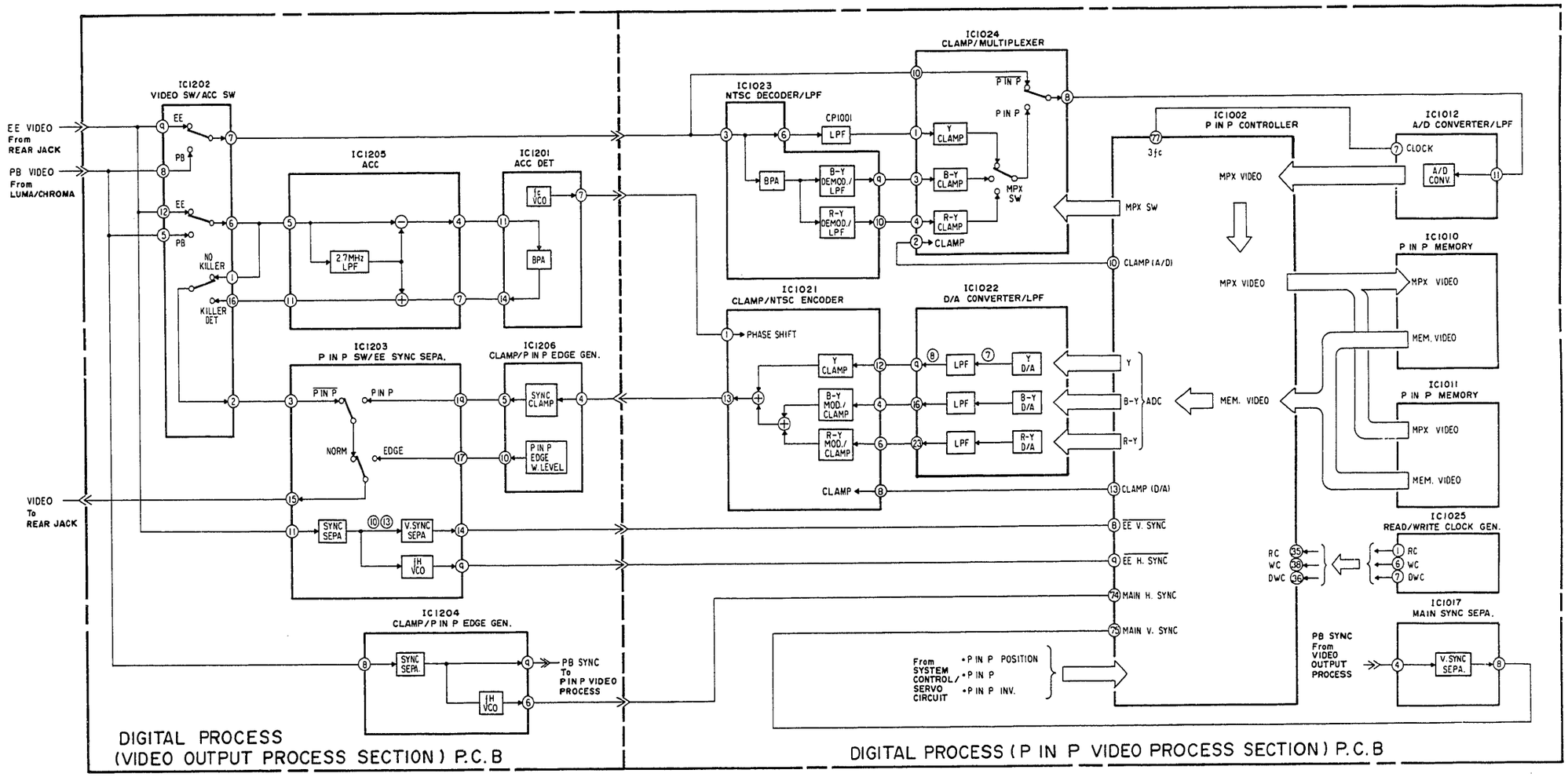


Fig. 1-3 P IN P Overall Block Diagram

– P IN P Edge Generator (IC1206) –

Generates a DC voltage equivalent to 100% white level to provide the borders between the main screen and sub-screen and applies it to the P IN P edge switch.

– E-E Sync Signal Separator (IC1202) –

Separates the horizontal and vertical sync signals from the video signal of the built-in tuner output or the line input and applies them to the P IN P controller. Receiving these signals, the P IN P controller times the writing of the E-E video signal and the reading of the playback signal to/from the P IN P memory.

– Main Sync Separators (IC1204, IC1017) –

Separate the horizontal and vertical sync signals from the video signal output from the luma/chroma circuit and apply them to the P IN P controller. Receiving these signals, the P IN P controller times the writing of the playback video signal and the reading of the E-E video signal to/from the P IN P memory.

1-4. P IN P Controller (See Fig. 1-4)

The P IN P controller is connected to the system control μP (abbreviated to the SμP hereafter) via three control signal lines (P IN P POSITION, P IN P INV, P IN P). To generate these control signals, the SμP receives one key input (P IN P button on the keyboard of the VCR) via the timer μP and two key inputs (P IN P and P IN P POSITION buttons on the keyboard of the remote control unit) via the tuning μP and timer μP.

The P IN P button sets/resets the P IN P mode and inverts the video signals of the main and sub-screens. This key input determines the outputs at pins 56 and 57 of the SμP.

Pin 56 "P IN P INV." is a control output to invert the video signals of the main and sub-screens; it goes "Hi" when the playback output is selected for the sub-screen and goes "Lo" in other modes (tuner or line input).

Pin 57 "P IN P" is a control output to set the P IN P controller to the P IN P mode; it goes "Hi" in the P IN P mode and goes "Lo" in other modes.

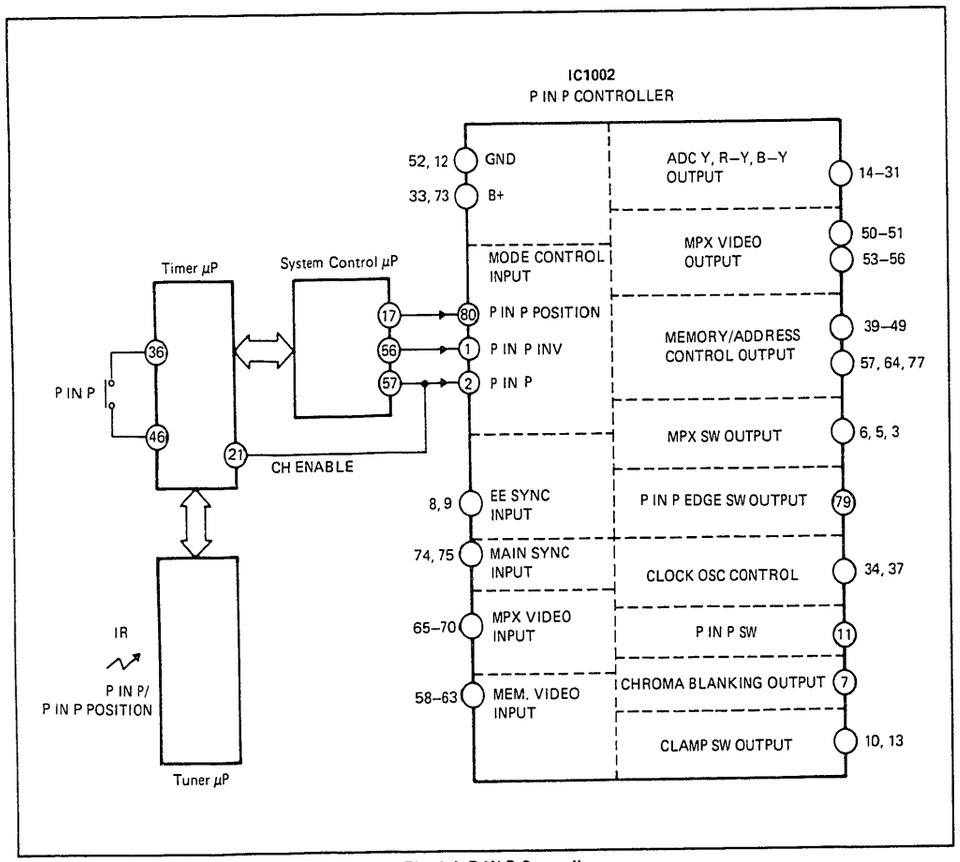
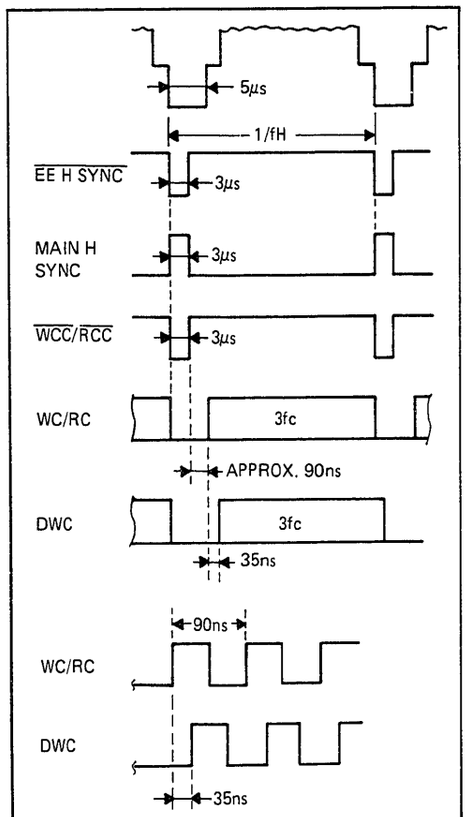


Fig. 1-4 P IN P Controller

The P IN P POSITION button shifts the position of the sub-screen frame to one of 4 corners on the main screen in the counterclockwise direction. This key input causes the SμP to generate a one-shot pulse with the width of 2.25 ±0.75 ms at pin 17 "P IN P POSITION".
The P IN P controller inputs the above 3 control signals and system-controls the whole P IN P circuit. The detailed operations will be described later for each item.

1-5. Clock Signal Generator (See Fig. 1-5.)

The P IN P controller provides three-phase clock signals (WC: Write Clock, RC: Read Clock, DWC: Delayed Write Clock) to process writing and reading of the sub-screen in real time asynchronously. The WC, DWC and RC signals are generated by CR oscillation circuit IC1025 and are input to pins 38, 36 and 35 of the P IN P controller. The WC and DWC signals at pins 38 and 36 are used to generate the control signals necessary to write sub-screen data to the P IN P memory, and the RC signal at pin 35 is used to generate the control signals to read the sub-screen data from the P IN P memory, in synchronizing with the scanning of the main screen. To synchronize the oscillation periods of these clock signals with the scanning of the main and sub-screens, the P IN P controller supplies two oscillation signals ($\overline{WCC}$: Write Clock Clear, $\overline{RCC}$: Read Clock Clear) at pins 37 and 34 to IC1025. The $\overline{WCC}$ signal at pin 37 and $\overline{RCC}$ signal at pin 34 are negative pulses with the width of 3 μs synchronized with the horizontal signals respectively separated from the sub and main screen video signals. IC1025 stops the oscillations of the RC and WC signals when the $\overline{WCC}$ or $\overline{RCC}$ signal is "Lo".



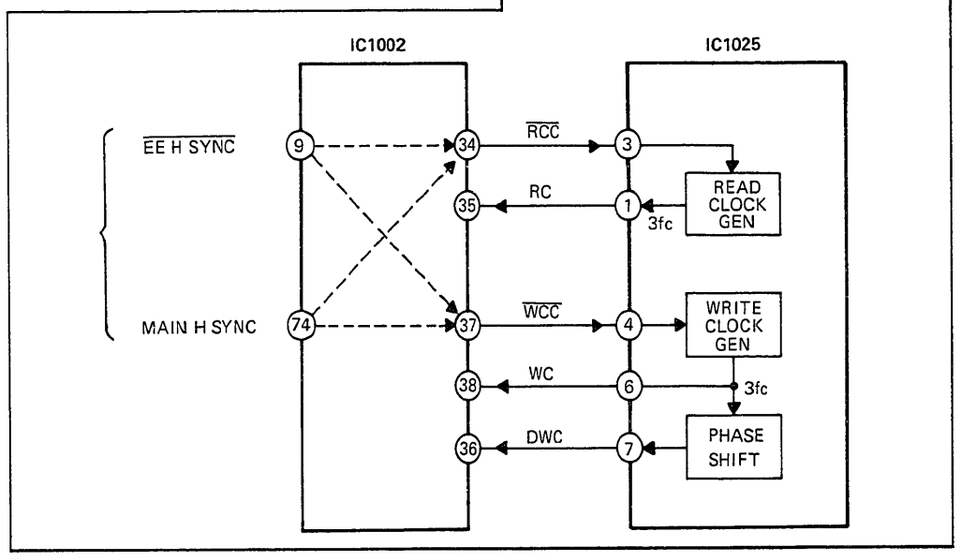
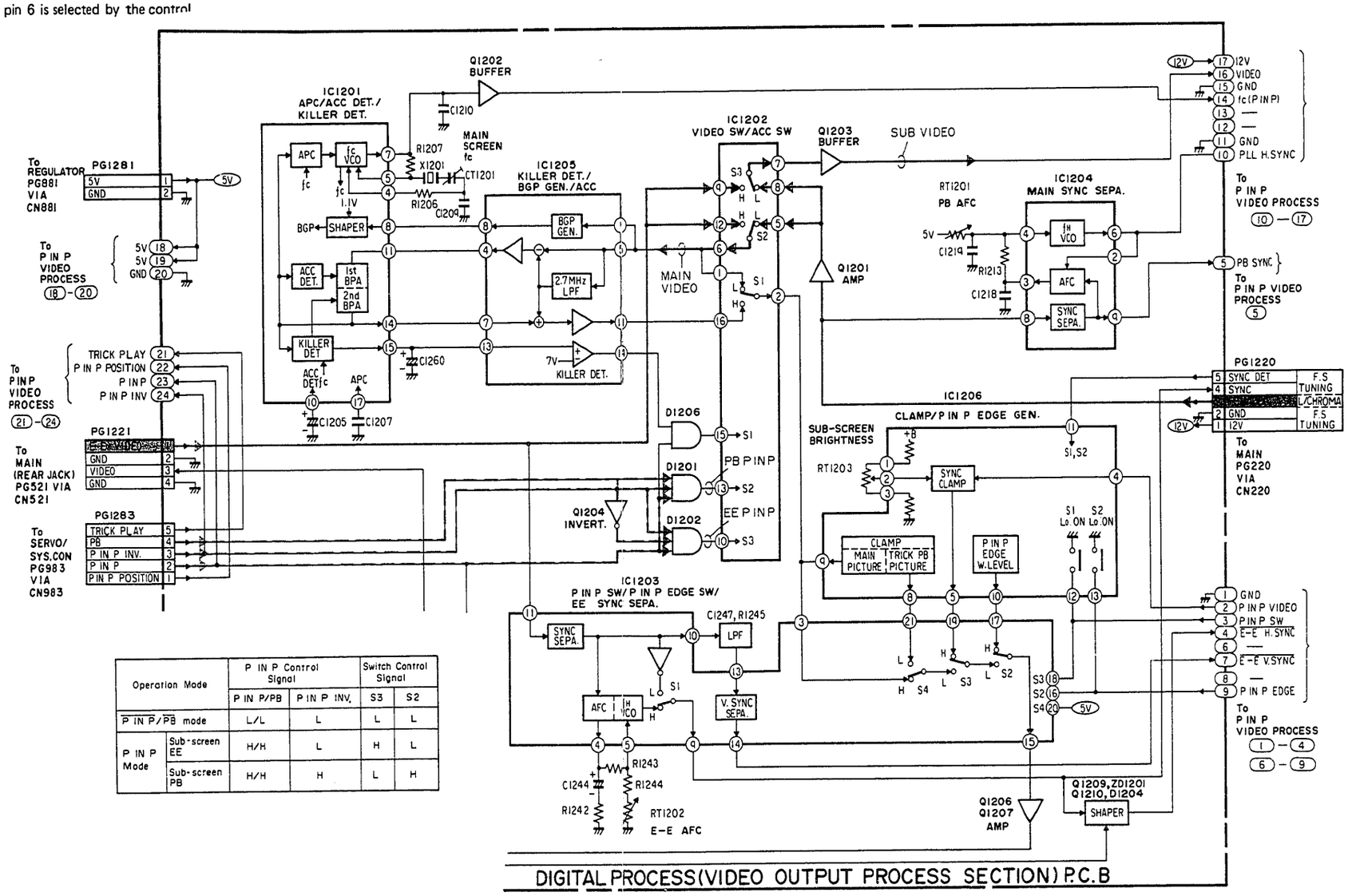


Fig. 1-5 Clock Signal Generator Circuit

1-6. Main/Sub Video Input Switch (See Fig. 1-6.)

The video signals supplied to the main/sub video signal processing circuit is changed over by the video input switch IC1202. IC1202 inputs the PB video signal from the luma/chroma circuit via pins 8 and 5 and the EE video signal from the tuner or video input jack via pins 9 and 12, and selects the video signal output to pins 7 and 6 using the switch control signals input to pins 10 and 13. The video signal at pin 7 is selected by the control signal at pin 10 and is supplied to the sub-screen video signal processing circuit. The video signal at pin 6 is selected by the control signal at pin 13 and is supplied to the main screen video signal processing circuit. The switch control signals at pins 10 and 13 are supplied from the switch control signal generator circuit consisting of Q1204, D1201 and D1202. The switch control signal generator circuit accepts three input P IN P control signals (PB, P IN P, P IN P INV.) described in the "P IN P controller" from the SμP and generates the switch control signals.



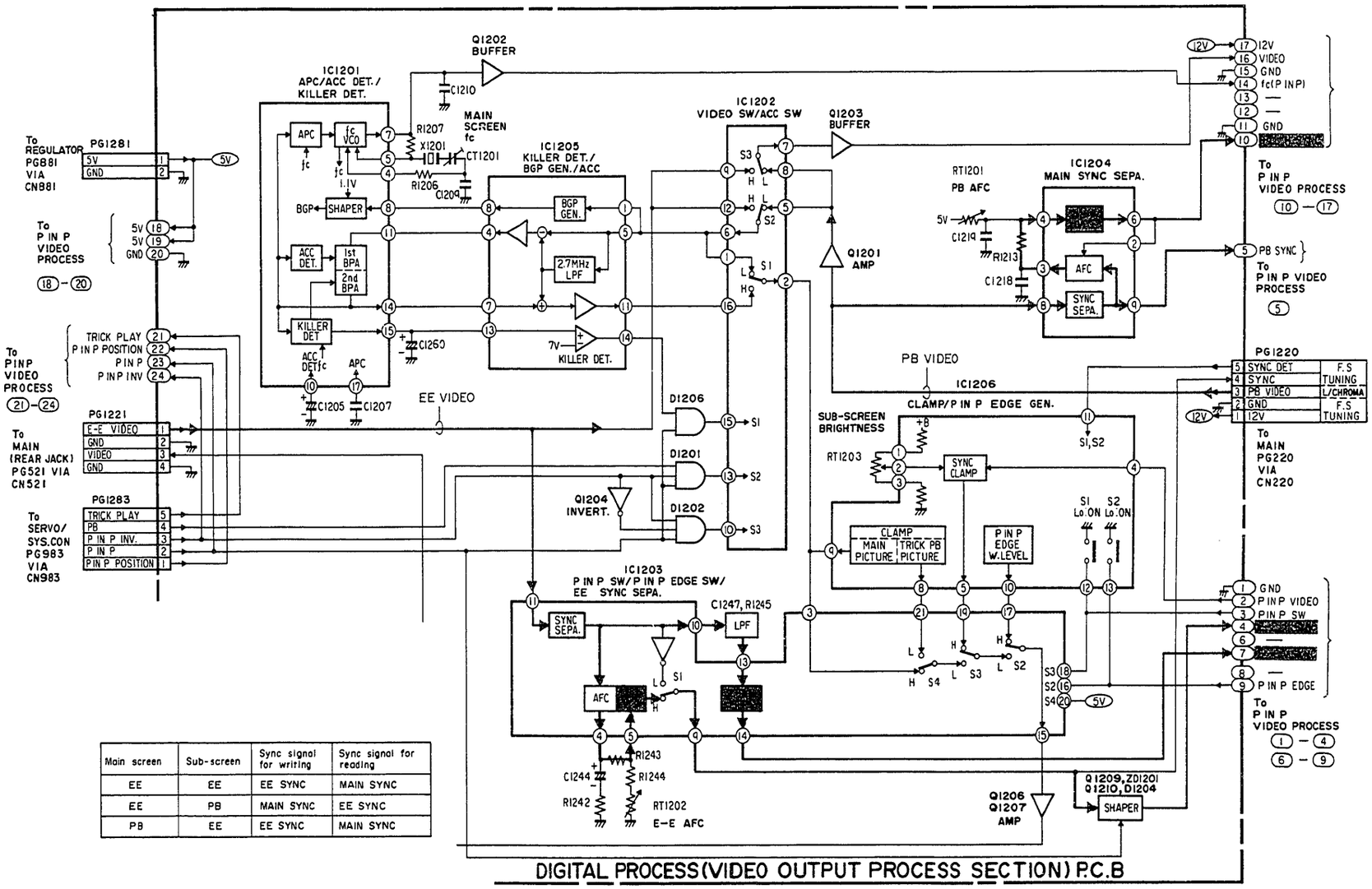
Operation Mode		P IN P Control Signal		Switch Control Signal	
		P IN P/PB	P IN P INV.	S3	S2
P IN P/PB mode		L/L	L	L	L
P IN P Mode	Sub-screen EE	H/H	L	H	L
	Sub-screen PB	H/H	H	L	H

Fig. 1-6 Main/Sub Video Input Switch Circuit

1-7. Sync Signal Separator (See Figs. 1-7 and 1-8.)

The sync signals necessary for the write/read control of the P IN P memory are separated from the video signal (called the "EE VIDEO") supplied from the built-in tuner or video input jack and the video signal (called the "MAIN VIDEO") output from the luma/chroma circuit The sync signal separated from the EE VIDEO signal is called the "EE SYNC" and the sync signal separated from the MAIN VIDEO signal is called the "MAIN SYNC". The EE SYNC signal is separated by sync separator IC1203 and the MAIN SYNC signal is separated by sync separator IC1204 and comparator IC1017. IC1203 separates the composite sync signal from the EE VIDEO signal input via pin 11 using the sync separator and supplies its output to the AFC circuit and pin 10. The AFC circuit together with the voltage-controlled oscillator (fH VCO) synchronizes the fH VCO oscillation frequency with the horizontal sync signal separated from the composite sync signal. Through this sync operation, a horizontal sync signal (EE H SYNC) without an equalizing pulse and external noise is obtained.

To synchronize the fH VCO oscillation output with the horizontal sync signal separated from the composite sync signal, the AFC circuit detects the frequency error voltage between these signals and outputs it at pin 4. The output voltage is divided by R1243, R1244 and RT1202 and is fed back to the fH VCO to correct the oscillation frequency of the fH VCO. RT1202 adjusts the free-run frequency of the VCO to 15,736 Hz (fH). The EE H SYNC signal passes through switch S1 and the shaper circuit and is supplied to the P IN P controller via pin 9. S1 always selects the fH VCO output because the switch control input at pin 8



Main screen	Sub-screen	Sync signal for writing	Sync signal for reading
EE	EE	EE SYNC	MAIN SYNC
EE	PB	MAIN SYNC	EE SYNC
PB	EE	EE SYNC	MAIN SYNC

Fig. 1-7 Sync Signal Separator Circuit

is fixed at 5 V. The shaper operates in the P IN P mode and shapes the EE H SYNC signal waveform so that its leading edge and trailing edge are steep. Since this results in external noise not being superimposed on the leading and trailing edges of the EE H SYNC signal, the fluctuations in the edge lines of the sub-screen due to external noise are prevented.

The composite sync signal at pin 10 of IC1203 is integrated by the integration circuit consisting of C1247 and R1245 and is shaped to a square wave by the vertical sync separator circuit in IC1203 and is then supplied to the P IN P controller via pin 8.

IC1204 and IC1017 together separate the MAIN H SYNC and MAIN V SYNC signals from the MAIN VIDEO signal in the same way as the above-mentioned IC1203. The MAIN H SYNC and MAIN V SYNC signals are output from IC1204 pin 6 and IC1017 pin 8 respectively and are supplied to pins 74 and 75 of the P IN P controller.

It is judged whether the sync signals input to the P IN P controller are in an odd or even field, and then the sync signals time the P IN P memory control signals for writing and reading the sub-screen data to/from the P IN P memory. See the "P IN P memory" for details.

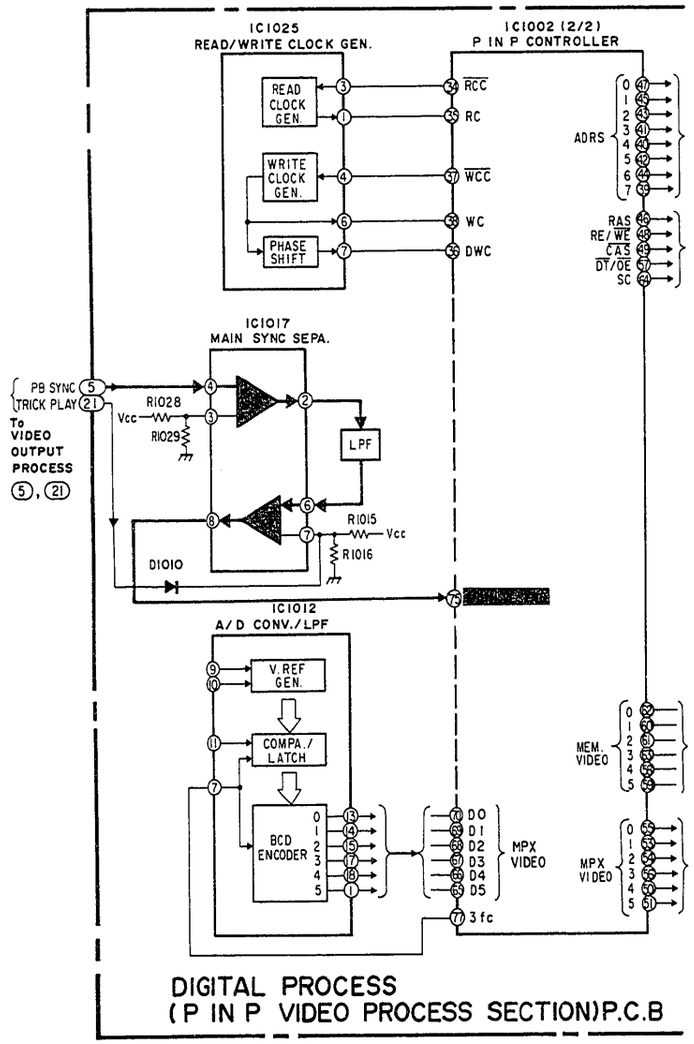


Fig. 1-8 Sync Signal Separator Circuit

1-8. Main Screen ACC Circuit (See Fig. 1-9.)

When the built-in tuner output or the video signal from the video input jack is selected as a main screen, the main screen ACC circuit always keeps the amplitude of the chroma carrier signal constant and generates a chroma subcarrier fc which is necessary to modulate the D/A converted R-Y and B-Y signals to a chroma signal.

This circuit consists of 4 ICs. IC1205 generates a burst gate pulse (BGP), shapes the killer voltage and limits the frequency band of the ACC. IC1201 performs the ACC, detects the killer voltage and executes APC. IC1202 is a switch which makes the main screen ACC circuit the THROUGH mode when a black and white signal is input. IC1206 clamps the output of the main screen ACC circuit. IC1205 generates the BGP signal necessary for IC1201, compensates the high frequencies of the luminance signal and performs ACC together with IC1201.

IC1205 and IC1201 play the following roles to generate BGP signals. To determine the phase of the BGP signal, the burst gate pulse generator (BGP GEN) in IC1205 separates the horizontal sync signal from the main screen video signal input via pin 1, delays it by approx. 0.25 μs and differentiates it and then supplies it to IC1201. To determine the pulse width of the BGP signal, IC1201 compares the BGP signal of differentiated waveforms supplied from IC1205 and the 1.1 V reference voltage at the shaper and converts the differentiated waveform to a square wave with a pulse width of approx. 3.5 μs.

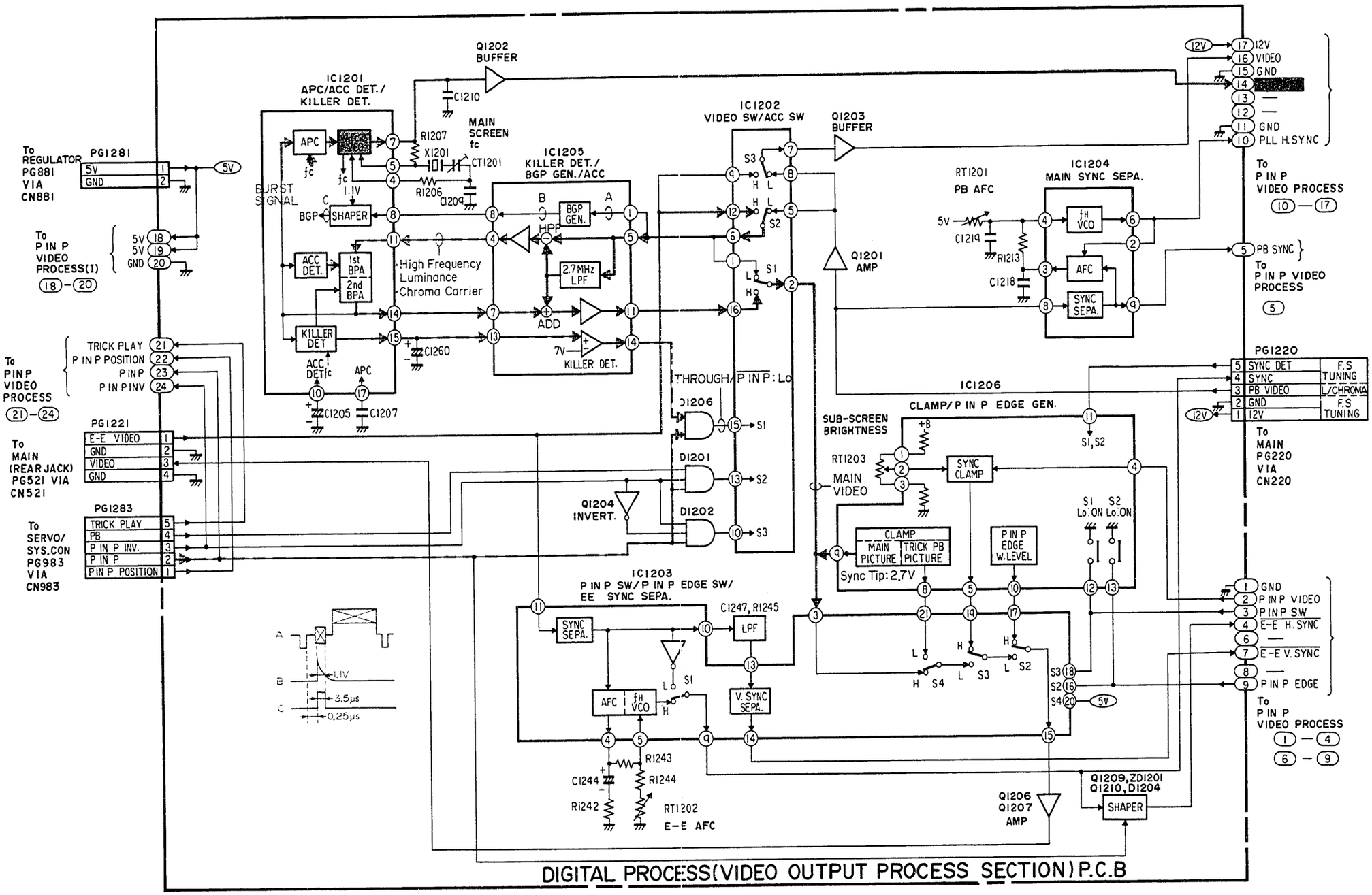
IC1205 and IC1201 also operate as follows to compensate the high frequency response of the luminance signal and perform the ACC function. In IC1205, the 2.7 MHz low-pass filter (LPF) and subtractor (-) form a highpass filter and separate the high-frequency components of the luminance signal and the chroma carrier signal components from the main screen video signal at pin 5 and supply them to IC1201. At the same time, IC1205 inputs the luminance signal with its high-frequency components compensated by IC1201 and also the chroma carrier signal which is controlled to be constant amplitude by IC1201 via pin 7 and applies these high-frequency components to the output of the LPF via the adder (+) and supplies them to switch IC1202.

IC1201 amplifies the high-frequency components separated from the main screen video signal at pin 11 using the first frequency-bandpass amplifier (1st BPA) and then applies the output to the second frequency-bandpass amplifier (2nd BPA). The 2nd BPA extracts the burst signal necessary for the ACC detector and amplifies it. The ACC detector detects the burst signal applied from the 2nd BPA and smooths it through capacitor C1205 at pin 10, and using the smoothed voltage, it determines the amplification of the 1st BPA. As a result, the amplitude of the chroma carrier signal is always controlled to be constant and the high-frequency components of the luminance signal are also compensated. This output is supplied to IC1205 via pin 14.

When a black and white video signal (video signal without burst signal) is input in the P IN P mode, the output of the main screen ACC circuit becomes a 2.7 MHz LPF output, that is only the low-frequency components, and if this is supplied to the TV as it is, the resolution drops. To prevent this, when a black and white signal is input, the main screen video signal is directly output bypassing the ACC circuit. These controls are performed by IC1201, IC1205 and IC1202. IC1201 performs killer detection through the killer detector (KILLER DET) and smooths the detected voltage via capacitor C1204 at pin 15 to supply it to IC1205. IC1205 compares the killer detection voltage at pin 15 of IC1201 and the 7 V reference voltage to generate a switch control signal and supplies it to IC1202. IC1202 inputs the ACC output via pin 16, the main screen video signal via pin 1 and the switch control signal via pin 15, and selects the video signal output at pin 2. When pin 15 is "Hi", the video signal at pin 16 is selected, and when it is "Lo", the video signal at pin 1 is selected. The switch control signal is obtained from pin 14 of IC1205 described previously through the AND circuit consisting of D1206. The AND circuit supplies the switch control signal from IC1205 to IC1202 only in the P IN P mode.

The output of the main screen ACC circuit is derived from IC1202 pin 2 and is supplied to the P IN P SW circuit after the clamper (CLAMP) at pin 9 of IC1206 clamps the sync tip of the main screen video signal to approx. 2.7 V.

The chroma subcarrier signal (fc) which is necessary to convert the D/A converted R-Y and B-Y signals to chroma signals is derived from the voltage-controlled oscillator (fc VCO) in IC1201. The fc VCO controls the fc VCO oscillation frequency, fc, so it has the same phase as the main screen burst signal together with the phase comparator (APC). The APC inputs the fc VCO output and the burst signal extracted by the 2nd BPA to detect the phase error voltage between them and smooths it through capacitor C1207 at pin 17. The smoothed phase error voltage is applied to the fc VCO to correct the VCO oscillation frequency. The VCO is oscillated by 3.58 MHz crystal oscillator X1201 connected to pins 4, 5 and 7 and the phase shifter (C1210, C1209, C1212, R1206, R1207).



DIGITAL PROCESS(VIDEO OUTPUT PROCESS SECTION) P.C.B

Fig. 1-9 Main Screen ACC Circuit

1-9. NTSC Demodulator, MPX, A/D Converter (See Figs. 1-10 and 1-11.)

This circuit consists of NTSC demodulator IC1023 which demodulates the video signal to its luminance and color-difference signals, IC1024 which clamps the luminance and color-difference signals within the sampling range of the A/D converter and converts luminance and color-difference signals to serial signals, IC1012 which converts the luminance and color-difference signals, converted to serial signals, to a digital signal quantized to 6 bits and the P IN P controller which controls these three ICs. IC1023 inputs the sub-screen video signal via pin 3 and operates the following.

- Generates the burst gate pulse (BGP) necessary to demodulate the color-difference signals.
- Separates the luminance signal and then limits the frequency band to less than half the sampling frequency.
- Demodulates the R-Y and B-Y color-difference signals and then limits the frequency band to less than half the frequency.

The generation method, phase and width of the BGP signal are the same as described in the main screen ACC circuit. The luminance signal is separated by the 1.3 MHz lowpass filter (LPF) at pin 6 and is limited to less than half the sampling frequency and is then applied to pin 1 of IC1024.

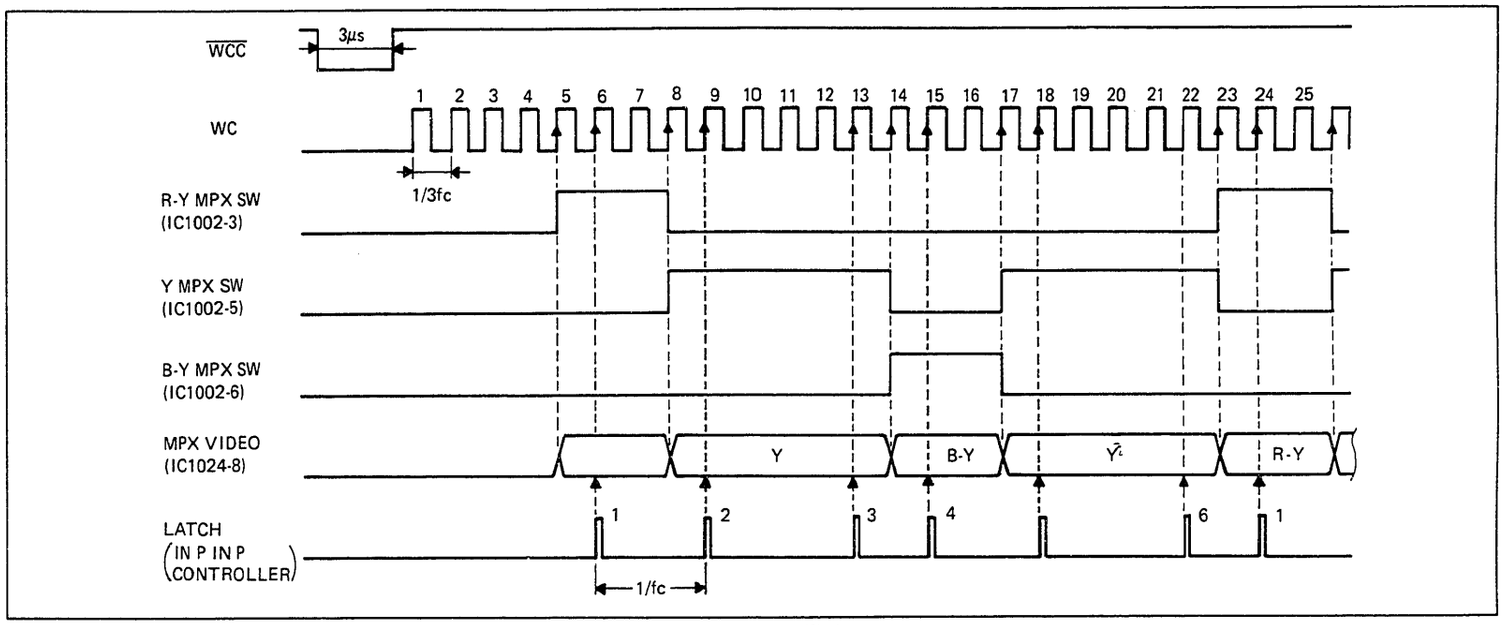


Fig. 1-11 MPX Operation Timing

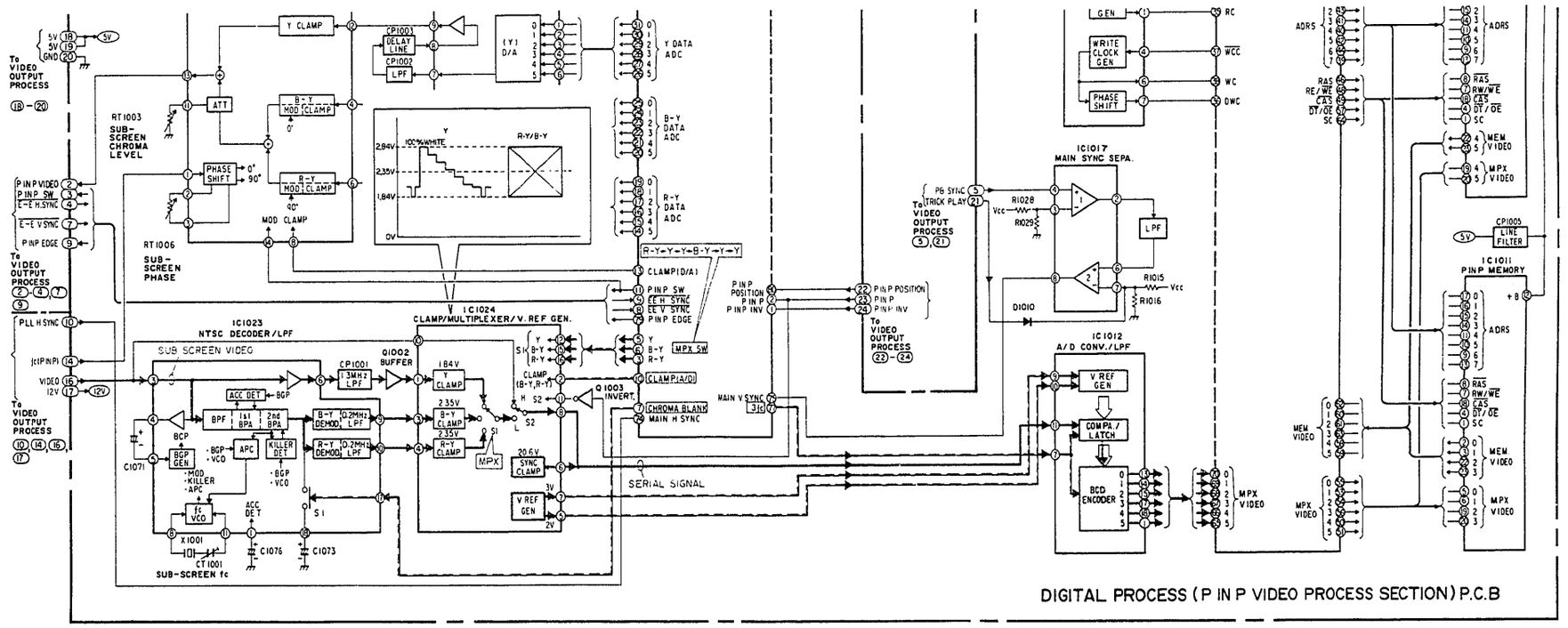


Fig. 1-10 NTSC Demodulator, MPX, A/D Convertor Circuit

The color-difference signals, B-Y and R-Y, are demodulated with the same processing as in a TV receiver. The demodulated color-difference signals are limited by the 0.2 MHz LPF to less than half the sampling frequency and are then applied to pins 3 and 4 of IC1024.

IC1023 stops the inputs to the demodulator circuit (R-Y DEMOD, DEB-Y MOD) to reduce noise on the pedestal lines (clamp points) of the color-difference signals in the horizontal retrace period. This is controlled by switch S1 connected to pin 18 and the P IN P controller. The P IN P controller generates the control signal (C. BLANK) of S1 using the sync signal separated from the video signal which is selected for a sub-screen and outputs it at pin 7. The phase of the C. BLANK signal is the same as that of the horizontal sync signal and its pulse width is determined to 12 μs equivalent to the horizontal retrace period. The C. BLANK signal turns S1 on. This causes the inputs of the demodulator (R-Y DEMOD, B-Y DEMOD) in IC1023 to be grounded via S1 and capacitor C1073 at pin 18. Therefore, noise on the pedestal line is reduced.

IC1024 inputs the luminance (Y) and color-difference signals (R-Y, B-Y) from IC1023 via pins 1, 3 and 4 respectively and operates the following.

- Sets the maximum amplitudes of each signal within the sampling range of the A/D converter using the clampers (Y CLAMP, R-Y CLAMP, B-Y CLAMP) corresponding to each signal.
- Converts each signal to serial signals using the multiplexer (MPX).
- Clamps the sync tip of the luminance signal equivalent to the minimum voltage of serial signal to a voltage which determines the minimum data of the A/D converter using the sync clamper (SYNC CLAMP).

The setting voltages of the Y, R-Y and B-Y CLAMPs are obtained by dividing 5 V by three ladder resistors (not shown). The sync tip of the luminance signal (Y) is set to 1.84 V by the Y CLAMP. The voltage of color-difference signals (R-Y, B-Y) corresponding to the sync tip period of the luminance signal is determined to 2.35 V, that is 0.5 V higher than the luminance sync tip level. Since the maximum amplitude of the Y signal is set to 1 V, half the voltage (2.35 V) of the maximum amplitude of Y signal becomes the clamp voltage of R-Y and B-Y signals. The clamp timing of the R-Y and B-Y signals is determined by the P IN P controller. The P IN P controller generates a clamp control signal (CLAMP A/D)) using the horizontal sync signal separated from the video signal which was selected for the sub-screen and outputs it at pin 10.

The CLAMP (A/D) signal is determined to a pulse with a width of 1 μs which is delayed from the trailing edge of the horizontal sync signal by 3.5 μs. This signal is supplied to the B-Y and R-Y CLAMPs via pin 2 of IC1024.

The multiplexer (MPX) inputs the clamped Y, R-Y and B-Y signals and selects them in sequence using the 3-phase MPX control signals supplied from the P IN P controller and converts them to serial signals. The P IN P controller generates the MPX control signals (Y MPX SW, B-Y MPX SW, R-Y MPX SW), synchronized with the horizontal and vertical sync signals separated from the video signal which was selected for the sub-screen, and outputs them at pins 5, 6 and 3. Sampling of the sub-screen is performed at the fc speed and the sampling order is determined as follows.

R-Y → Y → Y → B-Y → Y → Y

The Y signal is sampled much more because the frequency bandwidth of the R-Y and B-Y signals is approx. 1/4 the bandwidth of Y signal. The Y, R-Y and B-Y signals converted to serial signals are output at pin 8 via switch S2. S2 is controlled by the "P IN P" signal output from pin 57 of the system control μP and selects the MPX output in the P IN P mode (pin 57: Lo).

The setting voltage of SYNC CLAMP is determined to the minimum reference voltage (2 V) of the A/D converter described later. IC1012 inputs the Y, R-Y and B-Y signals converted to serial signals via pin 11 and converts them to digital signals quantized to 6 bits and then applies them to pins 65 to 70 of the P IN P controller.

The reference voltage necessary for A/D conversion is obtained from the reference voltage generator (V REF GEN) at pins 5 and 7 of IC1024 and the clock signal is from the P IN P controller. The V REF GEN generates the maximum and minimum reference voltages for A/D conversion. The minimum is determined to 2 V and the maximum to 3 V to cope with the maximum input amplitude, 1 Vp-p. These two reference voltages are applied to the reference voltage generator (V REF GEN) at pins 9 and 10 of IC1012, and the voltage (1 V) obtained by subtracting the minimum voltage (2 V) from the maximum voltage (3 V) is divided evenly to 1/64 by the ladder resistor. The voltages divided by 64 are applied to the comparator/latch circuit (COMPA/LATCH).

The COMPA/LATCH compares the MPX output voltage at pin 11 and the 64-step reference voltage applied from the V REF GEN when the clock signal equivalent to 3fc which is supplied from pin 77 of the P IN P controller is "Hi", and when the clock signal is "Lo", the COMPA/LATCH is set to a mode to latch the comparison result and applies the output to the BCD encoder.

The BCD encoder codes the comparison result of the COMPA LATCH to 6 bits and applies the outputs to pins 65 to 70 of the P IN P controller.

1-10. P IN P Memory
(See Figs. 1-12 and 1-13.)

The P IN P memory uses 2 chips on which of each 4 pairs of memory cell arrays of 256 x 256 bits are provided and allocates 6 pairs to each bit of the 6-bit digital sub-screen data. Since writing and reading of the digital sub-screen data must asynchronously be performed in real time and with the time axis converted, the P IN P memory provides a line buffer memory (LINE BUF MEM).

The LINE BUF MEM is in the P IN P memory, 1H-component data (256 bits) is transferred to the memory cell array when one address is designated and the transferred data is read by the serial clock exclusively for reading. Using this memory, writing to the memory cell array is performed every time the sub-screen is sampled (at the fc speed) by designating the address and data is transferred from the memory cell array to the LINE BUFF MEM every time horizontal scanning of the main screen is started (at the fH speed) by designating the address. Reading from the LINE BUF MEM is performed with the timing of the serial clock signal equivalent to 3fc and without the address designated. Since writing is performed at the fc speed and reading at 3fc, the time axes are shortened to 1/3 and the video signals of the 1/9 size sub-screen are generated. As the asynchronous clock signals are used for both writing and reading, different patterns can be selected for the main and sub-screens.

Since priority is given to reading from the memory cell array to LINE BUFF MEM over writing to the memory cell array, the P IN P controller has a temporary standby memory (STACK) for the written data. The STACK consists of 6 bits and each bit is allocated to 6 pairs of memory cell arrays. The STACK is triggered by the horizontal sync signal of the main screen to stack the data to be written to the P IN P memory temporarily for the 1/fc period and outputs it in the next cycle.

Since the sub-screen data with the same field as the odd or even field of the main screen and one field of which has been completely written must be applied to the main screen, the P IN P memory has an area in which the sub-screen data of 4 fields can be written for each 6 pairs of memory cell arrays. One field is uncomplete as writing is being done, and the other 3 fields to which writing is completed are selected according to the odd/even fields of the main screen and read. To detect the even/odd fields of both main and sub-screens, the P IN P controller detects the phase relations of the horizontal/vertical sync signals separated from both the main and sub-screen video signals to determine the odd or even field. The field detection output of the sub-screen determines the address of the field to which the sub-screen is written, and the field detection output of the main screen determines the address of the same field as the main screen and writing to which is completed.

The sub-screen data read from the LINE BUF MEM in the P IN P memory is converted in parallel to three signals, Y, B-Y and R-Y, by the demultiplexer (DEMPX) in the P IN P memory. Since the reading speed is three times the writing speed, the operation speed of the demultiplexer corresponds to this.

The P IN P memory uses a DRAM (Dynamic Random Access Memory) which needs rewriting (refreshing) of data within 4 ms after writing it. Since refreshing is performed in reading as well in writing, timing is determined so writing or reading to/from each memory cell array is performed within 4 ms in this unit. Therefore, the single refreshing operation is not performed.

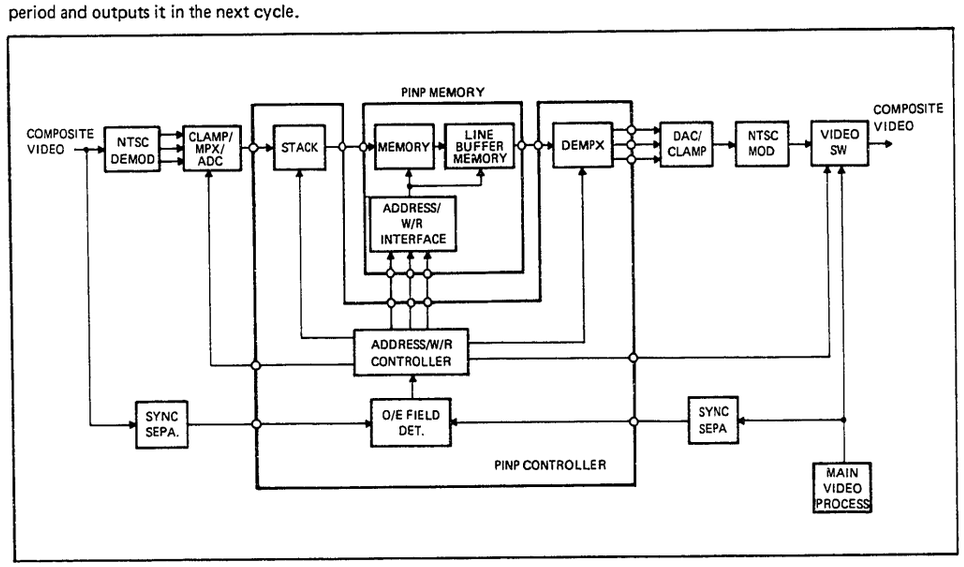
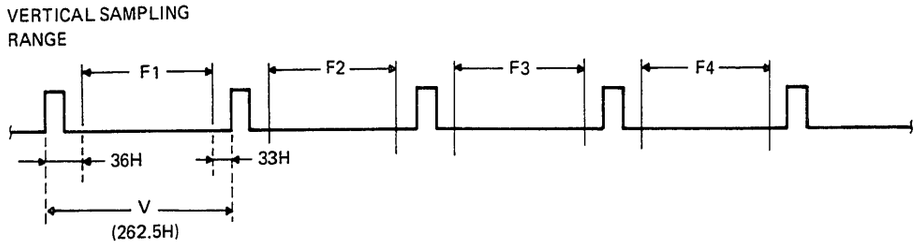


Fig. 1-12 P IN P Memory



H'

COL / ROW	LINE No	0	1	2	3	4	5	6		216		255
F1 0	19	R-Y	Y	Y	B-Y	Y	Y	R-Y				
1	22	R-Y	Y	Y	B-Y	Y	Y	R-Y				
63	208											
F2 64	282											
127	471											
F3 128	19											
191	208											
F4 192	282											
255	471											

Fig. 1-13 P IN P Memory Map

– P IN P Controller & P IN P Memory Connection (See Figs. 1-14 to 1-16.) –

Since data must be processed at the maximum speed of 3fc, a 6-bit parallel single-direction bus is used for data writing/reading and an 8-bit parallel single-direction bus is used for address data. As for the chip in which 6-bit digital sub-screen data is stored, LSB (2^0) to 4-bit (2^3) are allocated to IC1011 and the remaining bits (2^4, 2^5) are allocated to IC1010.

To control the writing of data on three data buses and to determine the operation mode of the P IN P memory, the P IN P controller applies the 5-bit control outputs ($\overline{RAS}$, $\overline{CAS}$, RW/$\overline{WE}$, SC, $\overline{DT}/\overline{OE}$) to the P IN P memories.

The RAS output determines the write timing of the row address data, write mode data and read mode data. The row address data, write mode data and read mode data are prepared on the address bus, RW/$\overline{WE}$ line and $\overline{DT}/\overline{OE}$ line respectively and are written to the P IN P memory when the $\overline{RAS}$ changes from "Hi" to "Lo".

The $\overline{CAS}$ output determines the write timing of the column address data. After the row address data is written to the P IN P memory, the column address data is prepared on the address data bus and is written to the P IN P memory when the $\overline{CAS}$ changes from "Hi" to "Lo".

The RW/$\overline{WE}$ output determines the write mode of the P IN P memory and the write timing of the sub-screen data. The P IN P memory has write-per-bit and random-write modes. In this unit the random write mode is used to write digital signals. The RW/$\overline{WE}$ must be held at "Hi" to set this write mode when the $\overline{RAS}$ changes from "Hi" to "Lo". After the row and column addresses are written to the P IN P memory, the sub-screen data on the write data bus is written to the P IN P memory when the RW/$\overline{WE}$ changes from "Hi" to "Lo".

The $\overline{DT}/\overline{OE}$ output determines the read mode of the P IN P emmory. There are data transfer and data read modes. In the data transfer mode, the 1 H data in the memory cell array is transferred to the line buffer memory. In the data read mode, the data on the line buffer memory is output to the outside of the chip. When the $\overline{RAS}$ changes from "Hi" to "Lo", the read mode is entered if the $\overline{DT}/\overline{OE}$ is held at "Hi" and the data transfer mode is entered if the $\overline{DT}/\overline{OE}$ is held at "Lo". In the read mode, the address data which is designated in the data transfer mode is read at the rise of the serial clock signal (SC) equivalent to 3fc. The data transfer mode is executed when the $\overline{RAS}$ and $\overline{CAS}$ change from "Lo" to "Hi" after the row and column addresses are designated.

The SC output is a serial clock signal equivalent to 3fc which is necessary to read data from the line buffer memory when the P IN P memory is set to the read mode. The data is read at the rise of the SC.

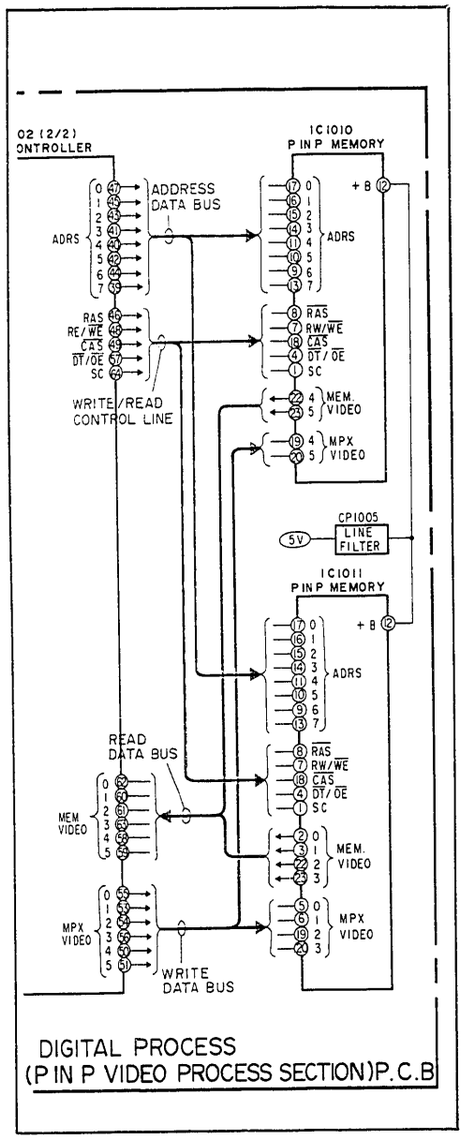


Fig. 1-14 P IN P Controller & P IN P Memory Connection

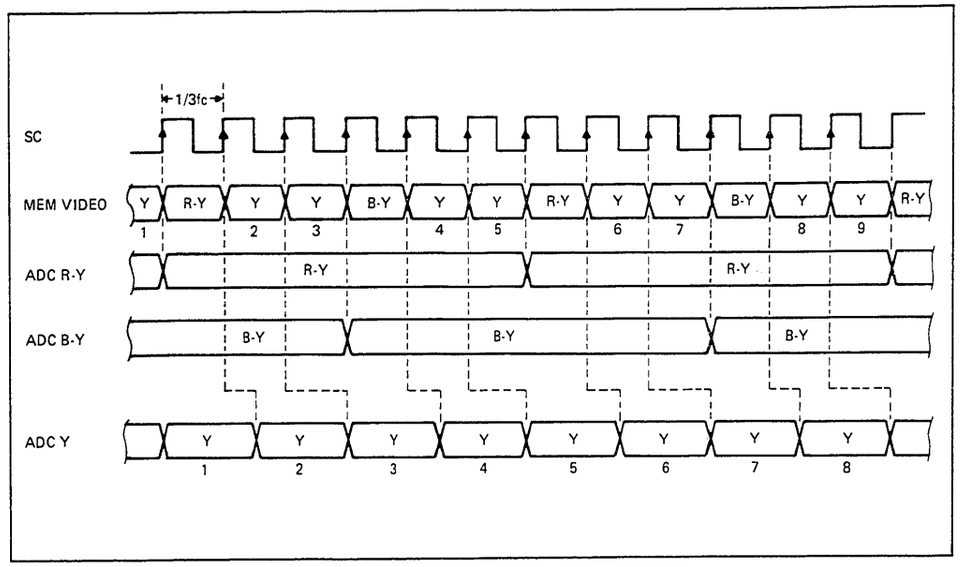


Fig. 1-15 Reading Timing Chart

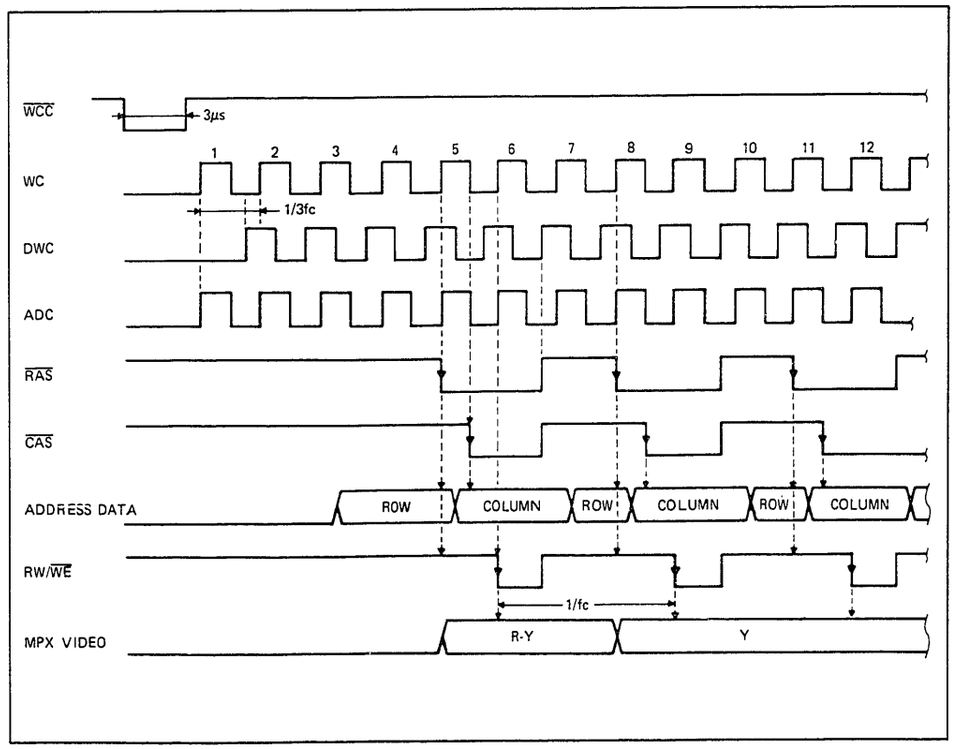


Fig. 1-16 Writing Timing Chart

1-11. D/A Converter/NTSC Modulator Circuits (See Figs. 1-17 and 1-18.)

This circuit consists of IC1022 which D/A converts the three signals and limits their frequency bands, IC1021 which modulates the three signals to an analog video signal and IC1206 which clamps the analog video signal.

IC1022 inputs the digital Y signals via pins 1 – 6, the digital B-Y signals via pins 10 – 15 and the digital R-Y signals via pins 17 – 22, and converts the digital signals quantized to 6 bits to an analog signal using separate exclusive D/A (Digital/Analog) converters.

The 3 MHz lowpass filter circuit (CP1002) limits the D/A converted Y signal to the specified frequency band and applies to the delay circuit (CP1003). CP1003 delays the D/A converted Y signal at pin 7 intentionally to compensate the delay of the D/A converted chroma signal due to the difference in the frequency bands between the Y signal and the R-Y/B-Y signals and matches the timings of the luminance and chroma signals.

The D/A converted R-Y and B-Y signals are limited by the lowpass filters (LPF) in the IC to the specified frequency band and are supplied to pins 4 and 6 of IC1021 respectively.

IC1021 clamps the B-Y and R-Y signals at pins 4 and 6 through the clampers (B-Y CLAMP, R-Y CLAMP) and modulates them to a chroma signal through the modulators (B-Y MOD, R-Y MOD). Then IC1021 adjusts the chroma signal to an optimum level through the attenuator (ATT) and resistor RT1003 at pin 11 and adds it to the luminance (Y) signal from pin 12 to create an NTSC video signal and outputs it at pin 13.

The setting voltages of the B-Y and R-Y CLAMPs are determined to 3 V respectively and the clamp timing is determined by the P IN P controller. The P IN P controller generates the clamp timing signal (CLAMP (D/A)) with the width of 1 μs approx. 2.8 μs after reading of the sub-screen data is started and outputs it at pin 13. This phase relationship is equivalent to the horizontal sync period in the video signal of the reduced sub-screen. The CLAMP (D/A) is supplied via pin 8 to the B-Y CLAMP and R-Y CLAMP in IC1021.

The B-Y MOD and R-Y MOD operate only while the sub-screen is framed to the main screen to reduce noise at the clamp points of the color-difference signals. This control is performed by the sub-screen position signal output from pin 11 of the P IN P controller described later. The B-Y MOD and R-Y MOD obtain the chroma subcarrier signal fc from the phase shifter to modulate the color-difference signals to a chroma signal. The phase shifter inputs the output of fc VCO described in "Main screen ACC circuit" via pin 1 and obtains the 0° and 90° phase-shift circuits. Resistor RT1006 between pins 2 and 3 adjusts the 90° phase-shift output correctly so that the tint of both main and sub-screens becomes the same when the same pattern is selected for both screens. The 0° and 90° phase-shift outputs are applied to the B-Y MOD and R-Y MOD respectively and are amplitude-modulated by the B-Y and R-Y signals. The outputs of the R-Y MOD and B-Y MOD are modulated by the balanced modulator (+) to chroma signals.

Resistor RT1003 at pin 11 adjusts the amplitude of the chroma signal so the saturation of the main and sub-screens is the same when the same pattern is selected for both screens.

When the same pattern is selected for the main and sub-screens, IC1206 uses the clamper (CLAMP) and aligns the sync tip of the sub-screen with that of the main screen to match the tones of both screens correctly. The CLAMP setting voltage is obtained at pin 2 by dividing the voltage between pins 1 and 3 by resistor RT1203. The CLAMP output is derived from pin 5 and is applied to the P IN P SW/P IN P EDGE SW circuits.

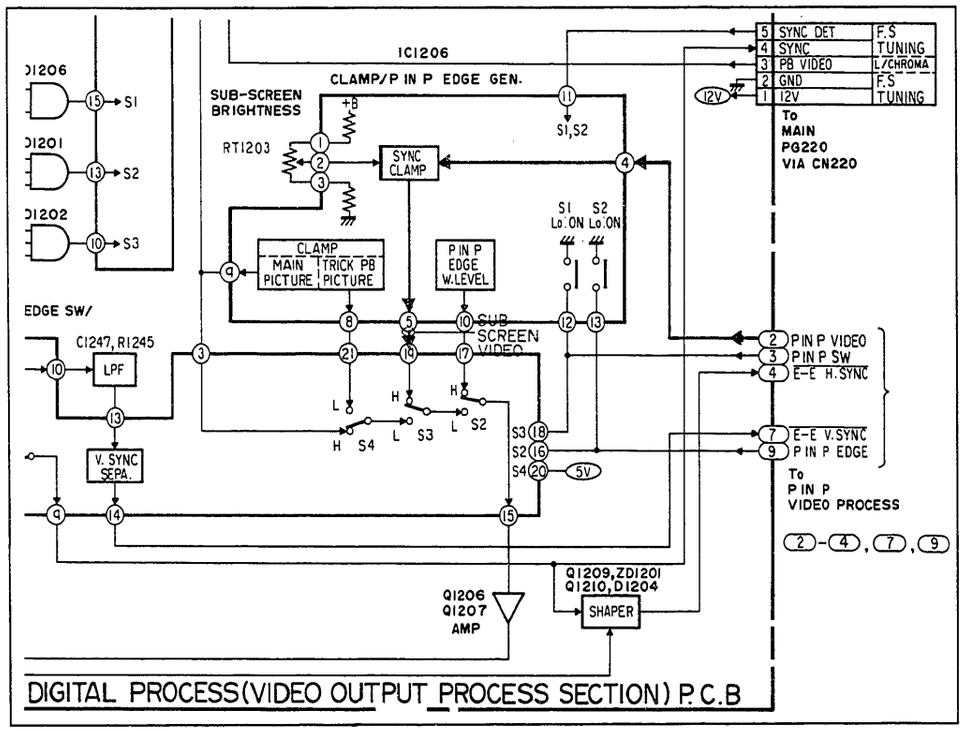


Fig. 1-17 D/A Converter, DEMPX, NTSC Modulator

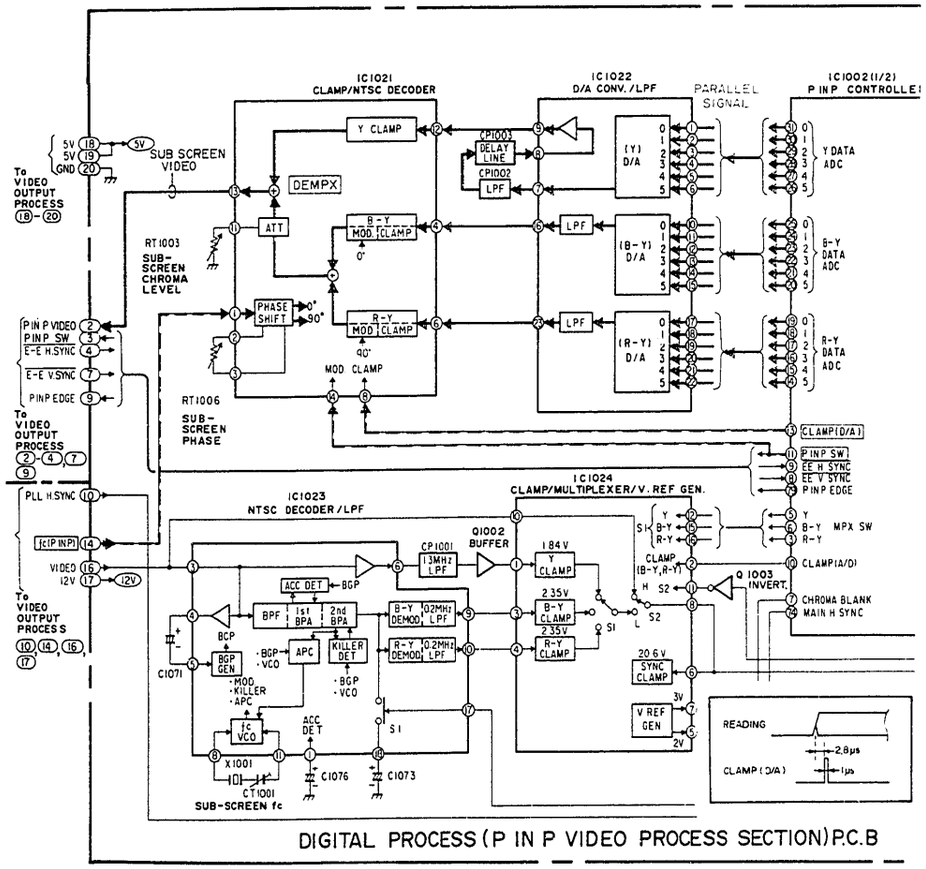


Fig. 1-18 D/A Converter, DEMPX, NTSC Modulator

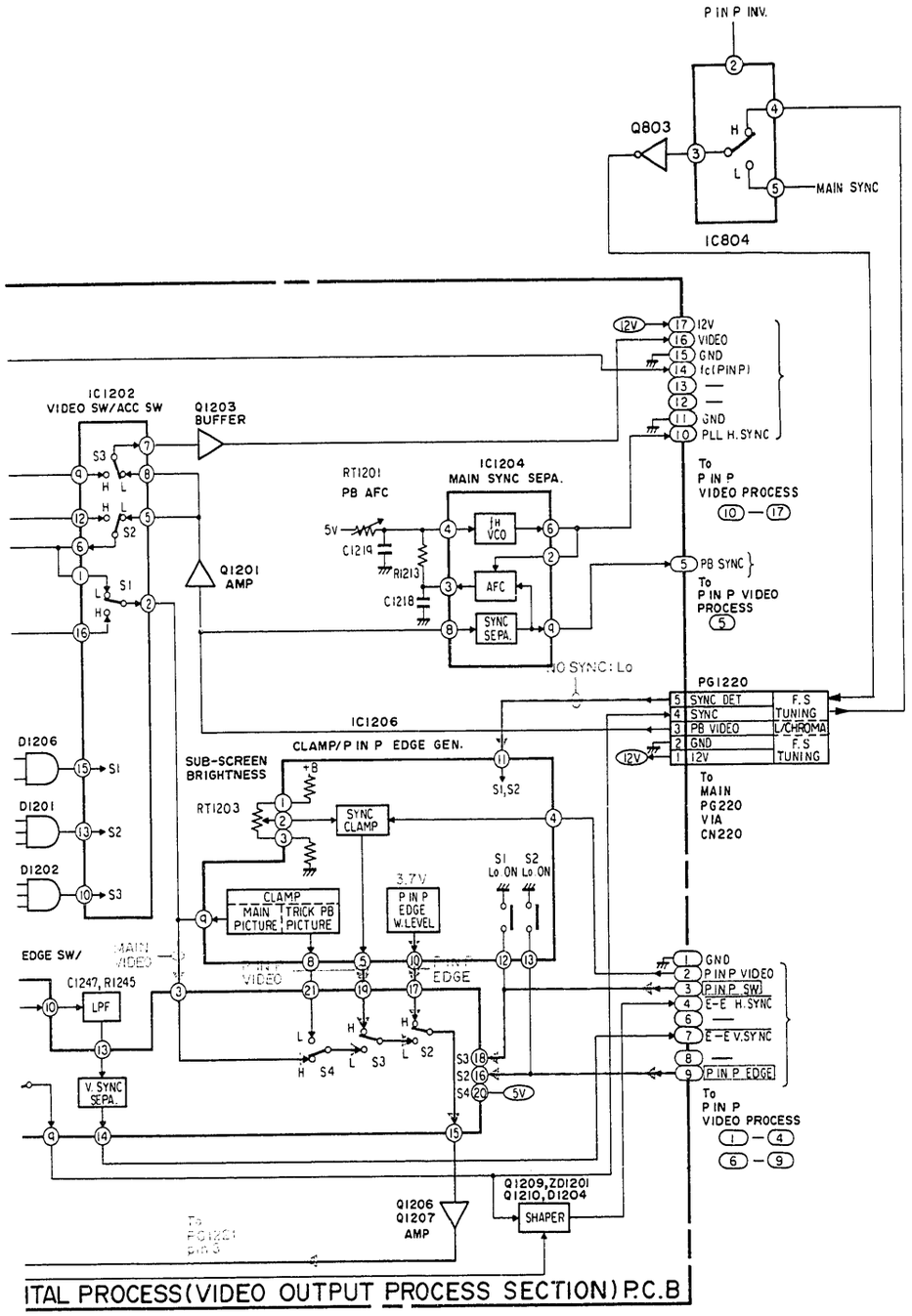


Fig. 1-19 P IN P SW/P IN P EDGE SW CIRCUIT

1-12. P IN P SW/P IN P EDGE SW Circuits (See Fig. 1-19.)

These circuits consist of IC1203 which performs replacement of the video signal, IC1206 which stops the sub-screen video output when the main screen video input is low or there is no input and generates an edge signal and the P IN P controller IC1002 which determines the positions of the sub-screen and edge lines.

IC1203 inputs the composite video signals of the main screen (MAIN VIDEO) and sub-screen (P IN P VIDEO) and the DC voltage for edging of the sub-screen via pins 3, 19 and 17 respectively and selects one of them according to one position of the 4 corners on the main screen in which the sub-screen is to be displayed (determined by the P IN P controller) and then outputs it at pin 15. The P IN P controller determines the read timing of the sub-screen data and the replacement timing of the video signals using the data of the sub-screen position on the main screen commanded by the operator and the sync signals separated from the main screen video signal. The P IN P controller generates two video signal replacement control signals (P IN P SW, P IN P EDGE SW) and outputs them at pins 11 and 79. The P IN P EDGE SW signal at pin 79 determines the timing to frame the sub-screen with edge lines. The widths of edge lines are determined to 1/fH vertical and 1/fc horizontal. The P IN P EDGE SW signal is supplied to P IN P EDGE SW S2 in IC1203. The P IN P SW signal at pin 11 of IC1002 determines the timing to frame the sub-screen with edge lines added to the main screen. The P IN P SW signal is supplied to P IN P SW S3 in IC1203.

IC1206 stops the framing of the sub-screen to the main screen when there is no sync signal separated from the main screen video signal. IC804 inputs the sync detection output from Q803 to PIN 11 of IC1206, and when there is no sync signal (PIN 11: Lo), it grounds pins 12 and 13 via the internal switch. Since this makes the outputs at pins 11 and 79 of the P IN P controller "Lo" forcibly, the framing of the sub-screen is stopped.

IC804 switches the sync signal applied to IC206 according to the video signal (EE or PB) selected for the main screen. This switching signal is produced by the "P IN P INV" signal output from the system control μP.

IC1206 (1/2) generates a DC voltage equivalent to 100% white level as an edge signal and outputs it at pin 10. This voltage is determined to approx. 3.7 V by adding 1 V to the clamp voltage, 2.7 V, of the main screen video signal.

The video signal at pin 15 of IC1203 which is obtained by framing the sub-screen in the main screen is supplied to the RF converter and video output jack via the 6-dB amplifier (Q1206, Q1207) and buffer (Q501).

1-13. P IN P Controller IC (IC1002) Pin Specification

Pin	I/O	Active Level	Abbreviation	Function
1	I	H	P IN P INV.	Main/sub screen inversion mode input. When the played back picture is selected as a sub-screen in the P IN P mode, this pin switches the sync signals input from the E-E or playback system which determine the write/read timings to/from the P IN P memory according to this selection.
2	I	H	P IN P	P IN P mode input. This input sets the P IN P controller to the P IN P mode and makes its output ports active.
3	O	H	R-Y MPX SW	Address selection outputs for the multiplexer. Supply the address select signal to the multiplexer to convert the sub-screen video signal separated into luminance and color-difference signals and converted to a serial signal.
5	O	H	Y-MPX SW	
6	O	H	B-Y MPX SW	
7	O	H	C. BLANK	Color-difference signal input inhibit output. Supplies the inhibit control signal to the NTSC demodulator to inhibit the input of the color-difference signals in the burst signal period of the sub-screen video signal.
8	I	L	$\overline{\text{EE V SYNC}}$	E-E video sync signal inputs. When the E-E video signal is selected for the sub-screen, the timing of writing to the P IN P memory is synchronized with these sync signals.
9	I	L	$\overline{\text{EE H SYNC}}$	
10	O	H	CLAMP (A/D)	Clamp timing outputs. The output at pin 10 determines the clamp timing of the R-Y and B-Y signals before A/D conversion, and the output at pin 13 determines them after D/A conversion to align the reference voltages of the R-Y and B-Y color-difference signals after NTSC demodulation and before modulation.
13	O	H	CLAMP (D/A)	
11	O	H	P IN P SW	Sub-screen position output. Determines one of the 4 corners of the main screen in which the sub-screen is to be framed and the output timing using the sync signal separated from the main screen video signal.
14	O	H/L	ADC R-Y 5	Outputs of the digital R-Y signal quantized to 6 bits. These are the outputs read from the demultiplexer in the P IN P memory and converted to a parallel signal.
15	O	H/L	ADC R-Y 4	
16	O	H/L	ADC R-Y 3	
17	O	H/L	ADC R-Y 2	
18	O	H/L	ADC R-Y 1	
19	O	H/L	ADC R-Y 0	
20	O	H/L	ADC B-Y 5	Outputs of the digital B-Y signal quantized to 6 bits. Same as the ADC R-Y signal.
21	O	H/L	ADC B-Y 4	
22	O	H/L	ADC B-Y 3	
23	O	H/L	ADC B-Y 2	
24	O	H/L	ADC B-Y 1	
25	O	H/L	ADC B-Y 0	

Pin	I/O	Active Level	Abbreviation	Function
26	O	H/L	ADC Y 5	Outputs of the digital Y signal quantized to 6 bits. Same as the ADC R-Y signal.
27	O	H/L	ADC Y 4	
28	O	H/L	ADC Y 3	
29	O	H/L	ADC Y 2	
30	O	H/L	ADC Y 1	
31	O	H/L	ADC Y 0	
34	O	L	$\overline{\text{RCC}}$	Reset output of the read-out clock generator. When the main screen enters the horizontal sync period, this pin stops the operation of the read-out clock generator to inhibit reading from the P IN P memory for approx. 3 μs.
35	I	H/L	RC	Read-out clock signal input. Inputs a clock signal equivalent to 3fc from the read-out clock generator to read the digital sub-screen data from the P IN P memory.
36	I	H/L	DWC	Write clock signal inputs. These pins input a clock signal equivalent to 3fc from the RC clock signal generator to write the digital sub-screen data to the P IN P memory. The clock signal input to pin 36 is the 140° phase delayed clock signal input to pin 38.
38	I	H/L	WC	
37	O	L	$\overline{\text{WCC}}$	Reset output of the write clock generator. When the original sub-screen picture enters the horizontal sync period, this pin stops the operation of the write clock generator to inhibit writing to the P IN P memory for approx. 3 μs.
39	O	H/L	ADRS 7	P IN P memory address data outputs. The address data is sorted into rows and columns and consists of 8 bits for each. Writing of the row addresses is executed when the write control signal at pin 46 changes from "Hi" to "Lo", and writing of the column addresses is executed when the signal at pin 49 changes from "Hi" to "Lo".
40	O	H/L	ADRS 4	
41	O	H/L	ADRS 3	
42	O	H/L	ADRS 5	
43	O	H/L	ADRS 2	
44	O	H/L	ADRS 6	
45	O	H/L	ADRS 1	
47	O	H/L	ADRS 0	
46	O	L	$\overline{\text{RAS}}$	Row address data write/process mode designation output. Times the writing of 8-bit row address data and the writing/reading of the digital sub-screen data.
49	O	L	$\overline{\text{CAS}}$	Column address data write output. Times the writing of the 8-bit column address data.
48	O	L	RW/$\overline{\text{WE}}$	Sub-screen data write output. Times the writing of the digital sub-screen data. When pin 48 changes from "Hi" to "Lo", the digital sub-screen data is written to the P IN P memory.

Pin	I/O	Active Level	Abbreviation	Function
57	O	L	$\overline{DT/OE}$	Data transfer mode/read mode output. Determines the data output mode of the P IN P memory together with the output at pin 46. When the output level at pin 46 changes from "Hi" to "Lo", the P IN P memory enters the data transfer mode when this pin goes "Lo", and it enters the data read mode when this pin goes "Hi". In the data transfer mode, the data in the memory cell array is transferred to the memory buffer of 1H component. In the data read mode, the data in the memory buffer of 1H component is output for every bit (column) synchronized with the serial clock signal output from pin 64.
50	O	H/L	MPX VIDEO 4	Digital sub-screen write output. 6-bit digital sub-screen data written to the P IN P memory.
51	O	H/L	MPX VIDEO 5	
53	O	H/L	MPX VIDEO 1	
54	O	H/L	MPX VIDEO 2	
55	O	H/L	MPX VIDEO 0	
56	O	H/L	MPX VIDEO 3	
58	I	H/L	MEM VIDEO 4	Inputs of data read from the P IN P memory.
59	I	H/L	MEM VIDEO 5	
60	I	H/L	MEM VIDEO 1	
61	I	H/L	MEM VIDEO 2	
62	I	H/L	MEM VIDEO 0	
63	I	H/L	MEM VIDEO 3	
64	O	H/L	SC	Output of the clock signals to read data from the P IN P memory. Outputs a serial clock signal equivalent to 3fc necessary to read the data in the line memory buffer of the P IN P memory.
65	I	H/L	MPX VIDEO 5	Inputs of the digital sub-screen data from the A/D converter.
66	I	H/L	MPX VIDEO 4	
67	I	H/L	MPX VIDEO 3	
68	I	H/L	MPX VIDEO 2	
69	I	H/L	MPX VIDEO 1	
70	I	H/L	MPX VIDEO 0	
74	I	H	MAIN H SYNC	Input of the horizontal sync signal separated from the main screen. Times the change of the row address when reading the digital sub-screen data from the P IN P memory.
75	I	H	MAIN V SYNC	Input of the vertical sync signal separated from the main screen. Times the change of field when reading the digital sub-screen data from the P IN P memory.
77	O	H/L	ADC	Output of the 3fc clock signal for A/D conversion.
79	O	H	P IN P EDGE	Edging control output. Determines the edging timing from the position on the main screen in which the sub-screen appears and the sync signals separated from the main screen.

Pin	I/O	Active Level	Abbreviation	Function
80	I	H	P IN P POSITION	Sub-screen position change input. Receives the command which shifts the sub-screen counterclockwise to the next of the 4 corners of the main screen.
4			TEST	For the operation test of the P IN P controller and the power inputs.
32			TEST	
71			TEST	
76			TEST	
12			GND	
33			Vcc	
52			GND	
73			Vcc	

1-14. Digital Circuit Abbreviations

ADC B-Y	Analog-to-digital converted B-Y signal
ADC R-Y	Analog-to-digital converted R-Y signal
ADC Y	Analog-to-digital converted luminance signal
ADRS	Address
CAS	Column address strobe
C. BLANK	Chroma blanking
DRAM	Dynamic random access memory
DEMPX	Demultiplexer
DWC	Delayed write clock
DT/OE	Data transfer/Output enable
INC	Row counter increment
MEN	Memory
MEM VIDEO	Memorized video
MPX	Multiplexer
MPX VIDEO	Multiplexed video
O/E	Odd/Even field
P IN P	Picture in Picture
RC	Reading clock
RCC	Reading clock clear
RCR	Row counter reset
RAS	Row address strobe
RFR	Refresh control
SC	Serial control clock
WC	Write clock
WCC	Write clock clear
WE	Write enable

2. TRICK PLAY CIRCUIT

2-1. Outline (See Figs. 2-1 and 2-2.)

Since this unit employs a three-head system, a picture with reduced noise can be obtained using the CH-2 head and trick play head with the same azimuth in the still, frame advance and slow play modes. When the F.ADV button is pressed and held down, the simplified slow play mode is entered at approx. 1/30 normal playback speed. The slow play speed is 1/5. Both modes are performed by driving the capstan motor intermittently using an exclusive drive circuit.

When the PAUSE button is pressed during play, the VTR enters the still mode. The unit stops tape at one CH-2 video track, aligning it with the scanning period of the video heads, and plays it back. When the F.ADV button is pressed in the still mode, the VTR enters the frame advance mode and the motor is pulse-driven to advance the frames while this button is held down. When the button is released, the VTR enters the still mode.

When the SLOW button is pressed during play, the VTR enters slow motion play and advances frames at approx. 1/5 the normal play speed automatically. When the PLAY button is pressed in the slow motion mode, this mode is released. The slow motion play is the same as when the F.ADV button is held down but the methods in which it is set and released are different.

It is necessary to locate a CH-2 video track within the scanning period of the video heads and to minimize noise in the still, frame advance and slow motion modes. To do this, the video track (tape) is stopped just before the optimum stop position, then the position in which the PB horizontal sync signal starts to be missing (this is assumed to be the tape stop position) and the optimum stop position are compared and the motor is pulse-driven until both positions are aligned. This optimum stop position is set to each edge of the head switching (SW30Hz) signal.

The main servo circuit configuration is the same as in previous models. For the still, frame advance and slow control, the following circuits are added to this unit.

- Feed pulse generator
- Brake pulse generator
- Horizontal correct pulse generator
- Still-head switching pulse generator
- Feed speed switch
- Capstan speed/direction encoder

These added circuits are controlled by the system control μP IC901.

IC901 controls the following items.

- Determines the intermittent drive mode (still, frame advance and slow). When one of these trick play modes is entered, the phase control loop of the cylinder servo is switched off. Both the phase and speed loops of capstan servo are switched off. The intermittent driver IC609 is activated.
- Disables the 3-bit capstan speed/direction setting signals applied to capstan motor driver IC602 from IC901 in the intermittent drive mode. IC609 controls IC602 in place of IC901.

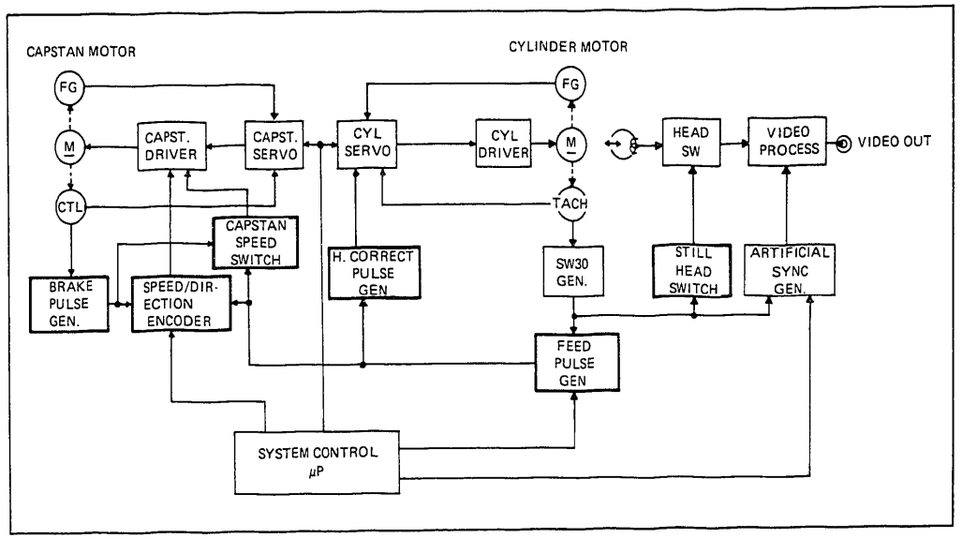


Fig. 2-1 Still/Frame Advance/Slow Control Block Diagram

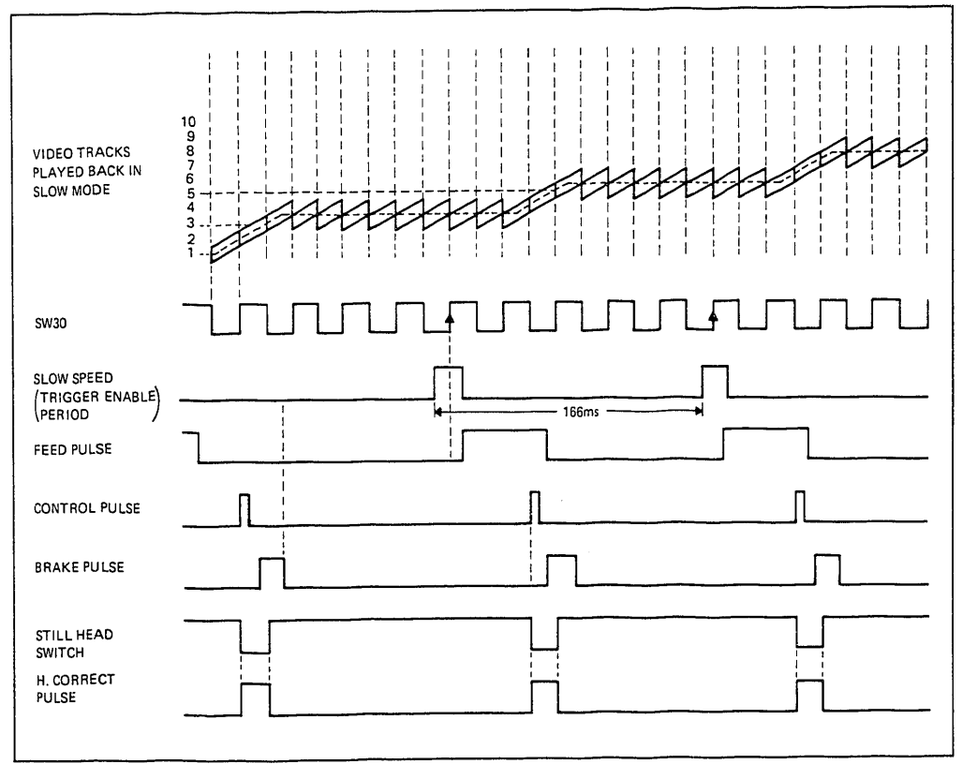


Fig. 2-2 1/5 Slow General Operation

2-2. Circuit Operations

2-2-1. System Control μP Outputs in Intermittent Drive (See Fig. 2-3.)

System control μP IC901 generates four control signals, SLOW, SLOW SPEED, LINE MUTE and F.SLOW in the intermittent drive mode. The SLOW signal is derived from pin 63 and is applied to pins 23 and 13 of IC601 and to pin 11 of IC609.

Receiving the SLOW signal, IC601 operates as as follows:

- Enters the pause mode because of the voltage (Vcc/2). This disables the cylinder phase loop and capstan speed/phase loops.
- Causes the gain setting input of the capstan drive voltage generating amplifier to be "Hi" due to the voltage (Vcc) at pin 13 and causes the capstan voltage to be "Lo".

The SLOW SPEED signal is derived from pin 60 of IC901 and is applied to pin 2 of IC609. This signal determines the slow speed and the number of frames to be advanced to 3 when the still mode is entered from play. The SLOW SPEED signal is a pulse-like output and the pulse width is approx. 2 ms and its period is 166 ms.

In the intermittent drive mode, IC609 triggers the slow speed pulse generator (described later) using the slow speed pulse. The LINE MUTE signal is derived from pin 42 of IC901 and is applied to pin 21 of audio processing IC403 and Q408 L/R to mute the audio signal. In the intermittent drive mode, the capstan speed/direction setting output pins 10, 11 and 12 are set to "Hi", "Lo" and "Lo" respectively. This means the "REC/PB" code.

Therefore, only the output at pin 10 is grounded via IC604. All pins 10, 11 and 12 go "Lo" (this means the "STOP" code), and the capstan speed direction setting outputs of IC901 are disabled.

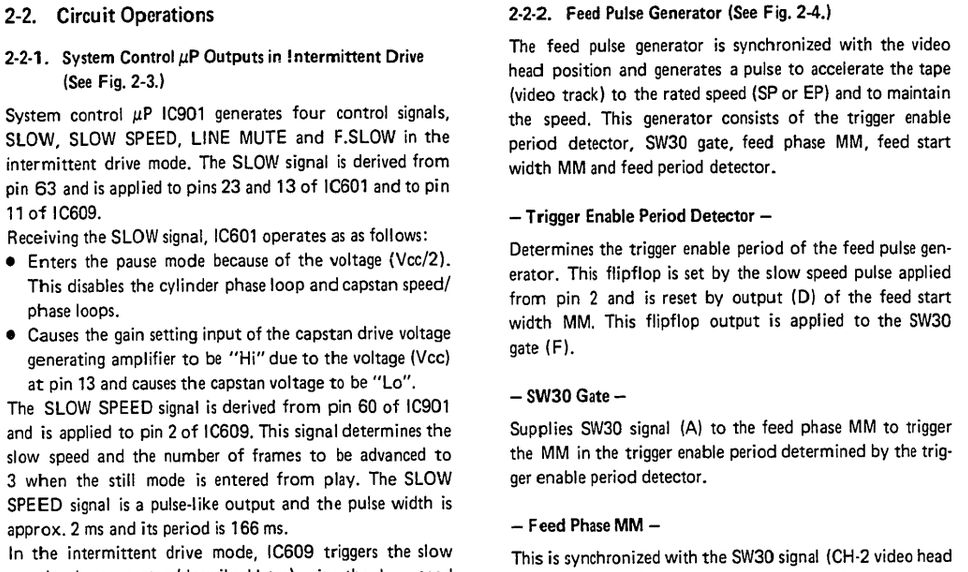


Fig. 2-3 System Control in Intermittent Driving Mode

2-2-2. Feed Pulse Generator (See Fig. 2-4.)

The feed pulse generator is synchronized with the video head position and generates a pulse to accelerate the tape (video track) to the rated speed (SP or EP) and to maintain the speed. This generator consists of the trigger enable period detector, SW30 gate, feed phase MM, feed start width MM and feed period detector.

– Trigger Enable Period Detector –

Determines the trigger enable period of the feed pulse generator. This flipflop is set by the slow speed pulse applied from pin 2 and is reset by output (D) of the feed start width MM. This flipflop output is applied to the SW30 gate (F).

– SW30 Gate –

Supplies SW30 signal (A) to the feed phase MM to trigger the MM in the trigger enable period determined by the trigger enable period detector.

– Feed Phase MM –

This is synchronized with the SW30 signal (CH-2 video head start information) to determine the appropriate start point of the tape (video track). This MM is triggered by the leading edge of the SW30 signal to generate pulse (C) the width of which is determined by the time constant (R687, C682) at pin 4 and applies this pulse to the feed start width MM.

– Feed Start Width MM –

Determines the acceleration period to accelerate the tape to the speed (SP or EP). This MM is triggered by output (C) of the feed phase MM and generates a pulse (feed start pulse: D) with the width determined by the time constant (R688, C683) at pin 6.

The output of this width MM is applied to the following three circuits.

- Trigger enable period detector:
  Resets this detector to determine the trigger enable period.
- Feed period detector:
  Described in detail later.
- Is output from pin 16 and is applied to the acceleration voltage switching input of the capstan speed switch (D). (Described in detail later)

– Feed Period Detector –

Sets capstan driver IC602 to "FF(S)" mode from acceleration end to deceleration start. This detector (flipflop) is set by feed start pulse (D) and is reset by brake pulse (E), and the pulse width is determined (G). The output of the feed period detector is derived from pins 13 and 19 and is applied to speed/direction setting input pins 10 and 12 of IC602. Application of output is equivalent to supplying the "FF(S)" code to IC602. IC602 drives the capstan motor forward at the speed determined by the speed setting voltage applied to pin 4. The speed setting voltage at pin 4 is controlled by the capstan speed switch described later and its level is determined matching the tape speed (SP or EP).

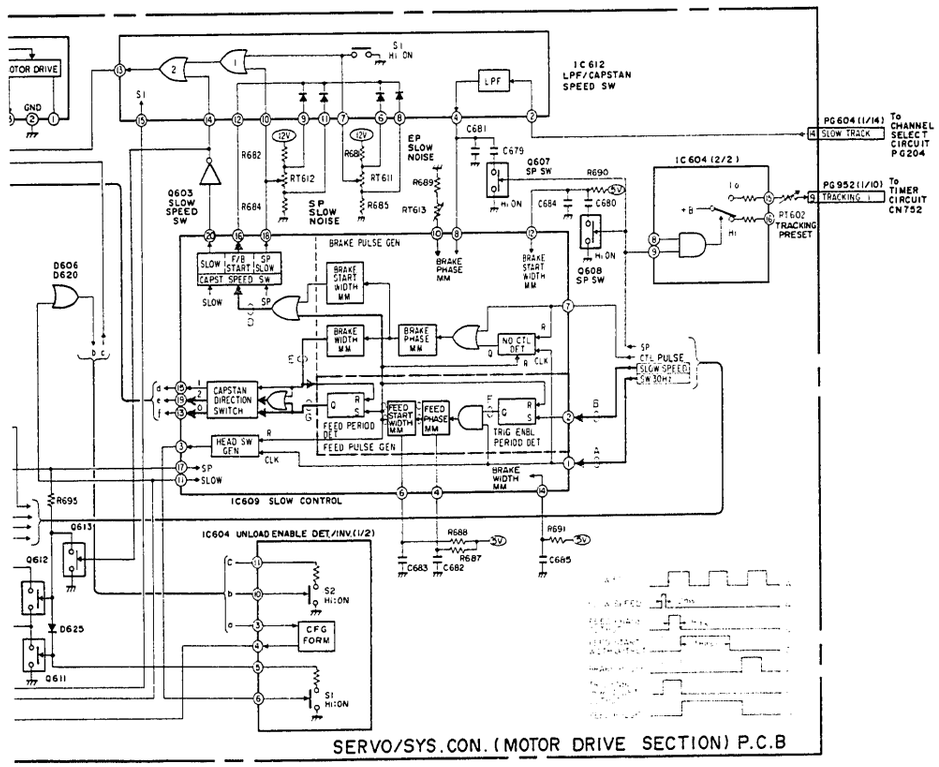


Fig. 2-4 Feed Pulse Generator

2-2-3. Brake Pulse Generator (See Fig. 2-5.)

The brake pulse generator is synchronized with the control pulse (CH-1 video track start information) just after the feed pulse is generated, and it generates a brake pulse to decelerate the tape and stop it so the next CH-2 video track position becomes appropriate.
This circuit consists of the brake phase MM, brake width MM, brake start width MM and No control pulse detector.

– Brake Phase MM –

Corrects the phase of brake pulse when the slow tracking control is operated by the user. This MM is triggered by control pulse (A) or the output of the No control pulse detector and generates a phase correction pulse (B) with the width determined by the time constant of C681 at pin 8 and RT613 and R689 at pin 10. RT613 at pin 10 adjusts the charge current flowing from pin 10 to C681 to fine tune slow pretracking. The output of the brake phase MM is applied to the brake start MM and brake width MM.

– Brake Width MM –

Determines the width of the brake pulse in the intermittent drive mode. This MM is triggered by output (B) of the brake phase MM and generates brake pulse (D) the width of which is determined by the time constant (R691, C685) at pin 14. The brake pulse is derived from pins 15 and 19 and is applied to speed/direction setting input pins 11 and 12 of IC602. Applying the brake pulse to pin 11 is the same as supplying the "REW(S)" code to IC602. The capstan is reversed (braked) by the speed setting voltage applied to pin 4. The voltage at pin 4 is supplied from the capstan speed switch described later.

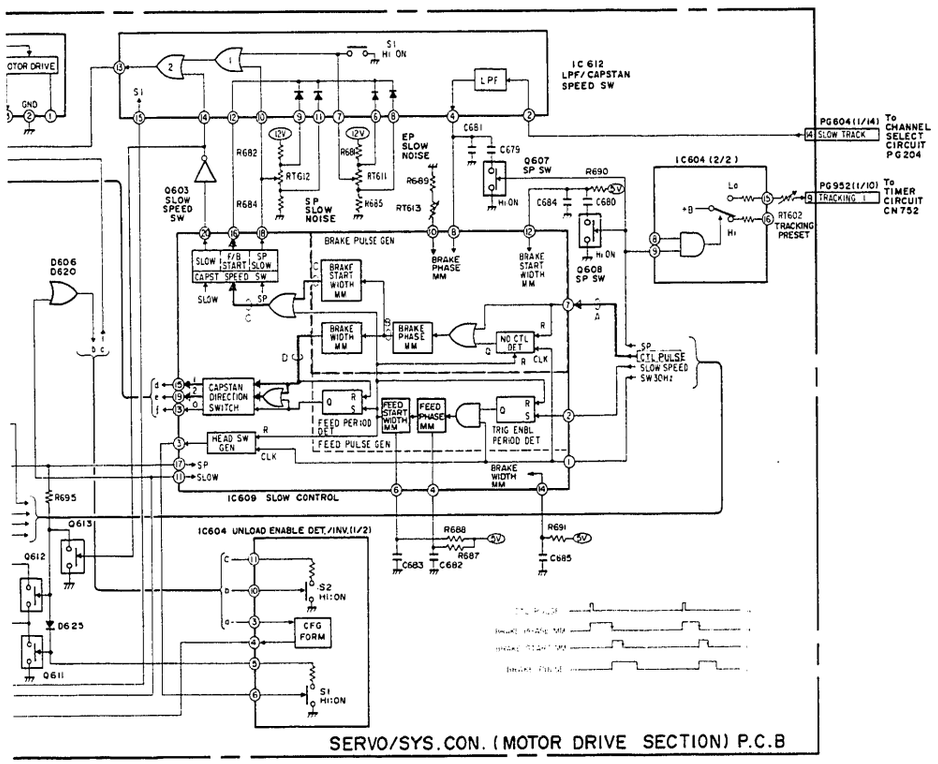


Fig. 2-5 Brake Pulse Generator

– Brake Start Width MM –

Determines the duration while a high voltage is applied to the speed setting input of IC602 to shorten the brake period. This MM is triggered by output (B) of the brake phase MM and generates a brake start pulse (C) the width of which is determined by the time constant (R690, C684) at pin 12. The brake start pulse is output at pin 16 and is applied to the capstan speed switch (C) described later.

– No Control Pulse Detector –

Monitors the control pulse just after a feed pulse is generated. If the control pulse is missing for a predetermined duration, this detector generates an artificial control pulse to trigger the brake pulse generator. This prevents the tape from being fed for several frames without being servo controlled. After the No control pulse detector is reset by the feed pulse described previously, it counts the period of the SW30 signal. When the control is missing for approx. 2 frames or more, the detector generates an artificial control pulse with a width of one field. This artificial control pulse is applied to the brake phase MM described previously to have the same effect as when a control pulse is input.

2-2-4. Capstan Speed Switch (See Figs. 2-6 and 2-7.)

This switches the speed setting voltage at pin 4 of IC602 which determines the capstan speeds are appropriate in the fast forward, rewind and intermittent drive modes according to the operation mode and tape speed (SP or EP). The FEED/BRAKE (F/B) START, SLOW and SP SLOW signals are output from pins 16, 20 and 18 respectively to select one of the possible speed setting voltages. The F/B START signal are produced by the pulses output from feed start width MM (A) and brake start width MM (D). This signal determines the duration in which the speed setting voltage is boosted to increase the driving or braking force at the acceleration or deceleration start.
The SLOW signal is inverted by Q603 and applied to IC612 pin 14. This signal determines the output duration of the speed control voltage necessary in the FF(S) and REW(S) modes when the slow mode is not set. In the FF(S) and REW(S) modes, since the $\overline{\text{CYL ON}}$ signal at pin 15 of IC612 goes "Hi" (1-1), S1 turns on to disable the voltage at pin 7. The voltage at Q603 is applied to IC602. The SP SLOW signal opens during SP slow and determines the output duration of the speed control voltage in the SP slow mode. Since the EP SLOW voltage from pin 7 is lower than the SP slow voltage, it is cut off by diode OR1.

2-2-5. Capstan Direction Switch (See Figs. 2-6 and 2-7.)

In the intermittent drive mode, the capstan direction control output applied from the system control μP to capstan motor driver IC602 is disabled. The capstan direction switch in IC609 controls capstan motor driver IC602 in place of the system control μP, thus controlling the capstan rotation direction.
Main servo IC601 is triggered by the PAUSE signal at pin 23 when the VTR enters the still mode to generate a brake signal at pin 16, the width of which is determined by the time constant at pin 17. This signal is supplied to IC602 pin 11 and IC604 pin 10 (2-1). This causes pins 10, 11 and 12 to go "Lo", "Hi" and "Lo" respectively, and this means that a REVERSE code is applied. Since the REVERSE code is applied for a short time, the capstan motor stops just before it turns in reverse. The voltages at capstan direction switch output pins 13, 15 and 19 are determined by the outputs of feed pulse generator (B) and brake pulse generator (C). Since pins 13, 15 and 19 go "Hi", "Lo" and "Hi" until the tape is decelerated after acceleration starts, IC602 is set to the FF(S) mode. These pins go "Lo", "Hi" and "Hi" respectively during the deceleration period and IC602 is set to the REW(S) mode.

2-2-6. Horizontal Correction Pulse Generator: Q611/Q612 (See Figs. 2-7 and 2-8.)

This generates a pulse to correct the horizontal frequency (fH) in the intermittent drive mode. Since the tape is wound around the cylinder just after the feed pulse is generated, the cylinder speed decreases and this causes the horizontal frequency to decrease. To correct this, the horizontal correction pulse generator is synchronized with the HEAD SW signal and generates a correction pulse, then applies it to the cylinder drive voltage.

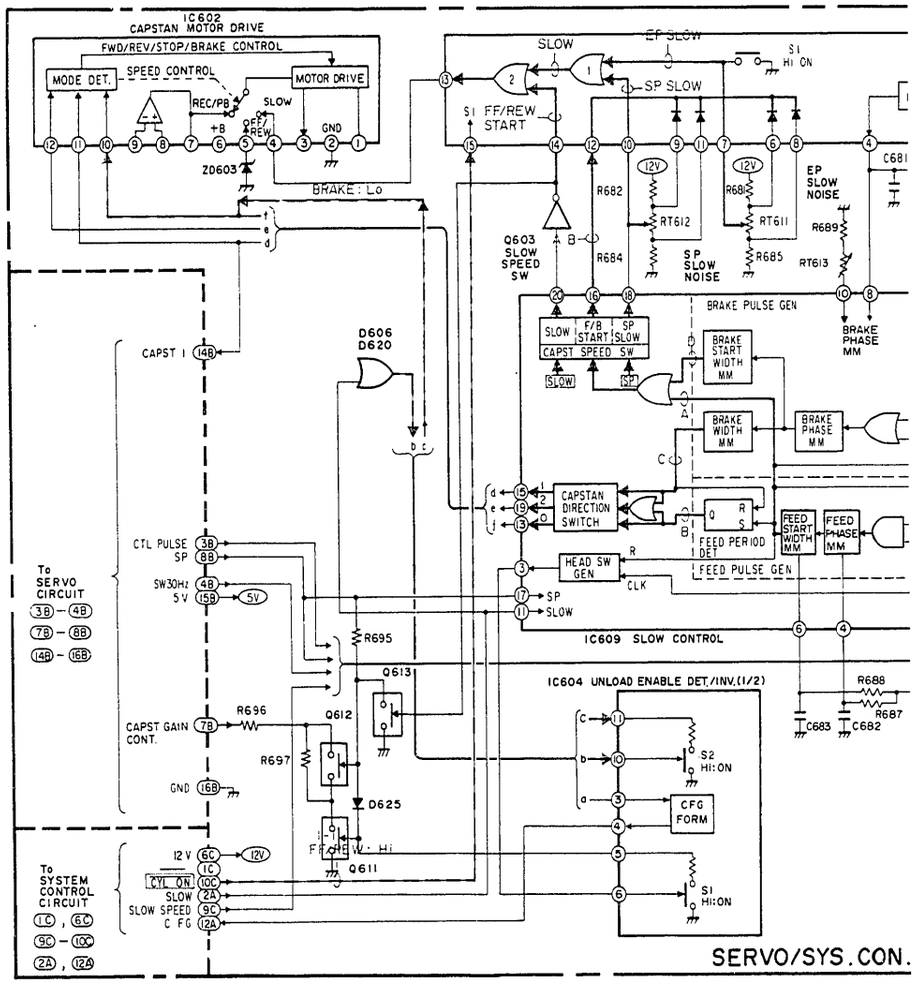


Fig. 2-6 Capstan Speed Switch/Direction Switch

Operation Mode		Speed Setting Voltage IC612-13 (IC602-4)	Switch Control (IC609)		
			F/B START (PIN 16)	SLOW (PIN 20)	SP SLOW (PIN 18)
FF(S)/REW(S)		4V	–	L	L
SP	F/B START	11V	L	H	H
	F/B	6V	H	H	H
EP	F/B START	4.4V	L	H	L
	F/B	3.4V	H	H	L

Note: F/B: FEED/BRAKE
FF(S)/REW(S): FF START/REW START

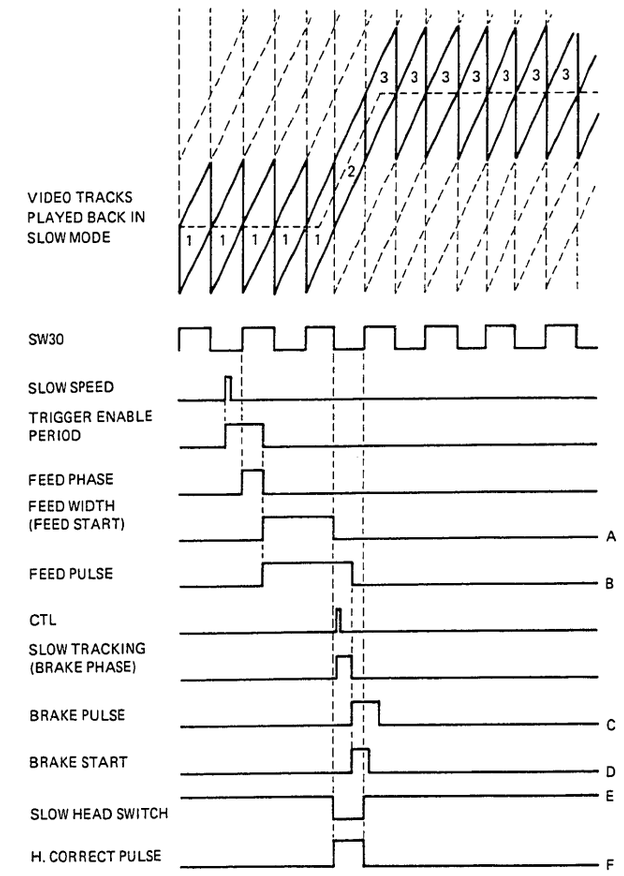


Fig. 2-7 Timing Chart of Slow Operation (APPENDIX)

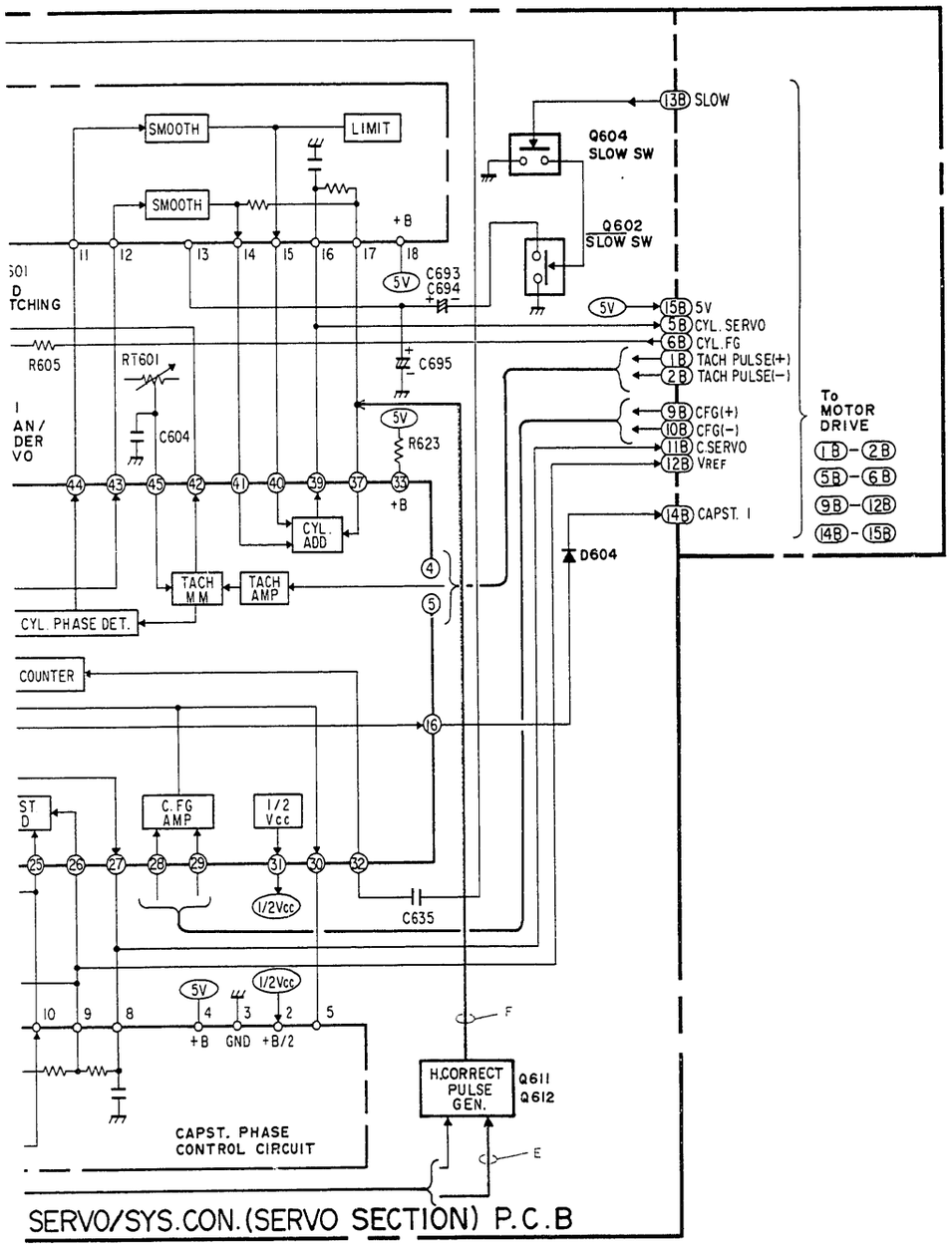


Fig. 2-8 H. Correct Pulse Generator

3. AUDIO CIRCUIT

3-1. Dolby-B System

Inherent in any audio tape recording process is background or hysteresis noise caused by the physical construction of the tape. In the VTR recording processes, this hysteresis or background noise occurs in the vicinity of 5 to 10 kHz. The background noise is normally not noticeable due to the level of the audio signals present. However, during very low level audio signals in the frequency range of the hysteresis noise, the hysteresis noise can become as great or possibly greater than any actual audio signal, thereby covering the audio signal with noise. The Dolby noise reduction system processes the audio signal to reduce the effects of the background noise by changing the dynamic range characteristics of the audio signal. There are several types of Dolby systems presently available ranging from very expensive commercial studio Dolby systems to consumer-type Dolby systems. This VTR utilizes the Dolby-B system which provides Dolby noise reduction in the frequency range of the hysteresis noise which is 5 to 10 kHz.
Best audio performance is achieved when recordings that were made with the Dolby circuitry turned "on" are played back with the circuitry "on" and likewise, recordings made without Dolby provide the best performance when played back with the Dolby processing turned "off". Playing back a non-Dolby recorded signal through a Dolby processing system causes the high level signals of the audio information to be larger or smaller than normal. Conversely, playing back a tape recorded with Dolby circuitry turned "off" causes the high frequency audio to be decreased in amplitude, thereby distorting the audio signal.

3-2. Audio Head Construction (See Fig. 3-1.)

The VHS standard permits an audio track width of 1 mm recorded on the very top edge of the video tape. This VTR plays the stereo audio information from this 1 mm track width. To accomplish this, the size of the two audio heads has been reduced to 0.35 mm each. This size reduction allows a spacing or guardband of 0.3 mm between the audio heads thereby providing excellent separation of the two audio signals.

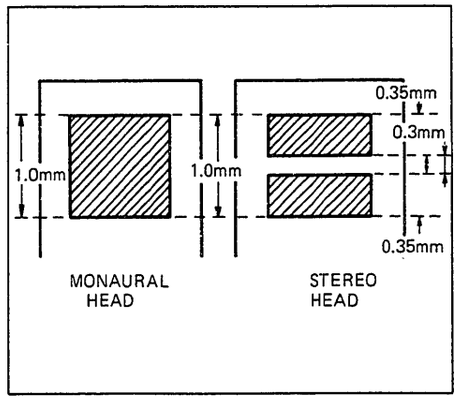


Fig. 3-1 Audio Head Construction

3-3. Dolby Switch Operation (See Fig. 3-2.)

Dolby ON/OFF operation is performed by the Dolby switch (S755) on the timer circuit board.
Dolby IC403 is located on the audio/MPX decoder circuit board; it contains 2-channel Dolby encoder/decoder to process both L-CH audio and R-CH audio.
IC403 performs Dolby processing when pin 25 is set to Hi. The Dolby switch is provided on the timer board together with the indicator; when it is turned on, the timer μP outputs Hi to

- light the indicator, and
- operate the Dolby NR circuit as an encoder (during recording)/decoder (during play).

3-4. EE/RECORD Operation (See Fig. 3-2.)

As with previous units, there are two possible input sources for audio information. These include the TV broadcast audio and the audio input jack audio. Both channel audio signals (line or tuner) are selected by input selector switch IC402 and are applied to IC403.

– Mode Setting –

(1-1 to 1-3), (2-1 to 2-7)
When the system control μP judges the record mode, PG442 pin 8 goes "Hi". (1-1)
This causes Q403 – Q405 to output "Hi" and this "Hi" is applied to:

- T401 to initiate bias oscillations. (1-2)
- Pin 24 of IC403 to activate the record amplifiers. (1-3)

Meanwhile, PG442 pin 3 goes "Lo". (2-1)
This causes Q406 to output "Hi". (2-2)
This "Hi" output is applied to pins 5 of IC401 L/R (2-3, 2-4) and terminates them with 10 ohms to configure the audio head in the record mode.
Q402 outputs "Lo" and this "Lo" output is applied to:

- Pins 7 of IC401 L/R (2-5, 2-6) to connect the record amplifiers and head.
- Pin 17 of IC403 (2-7) to set the record/playback switches (S1, S3 – S5) in the IC403 to the record positions.

– Input Selection –

(3-1 L/R, 3-2 L/R)
The tuner audio (3-1 L/R) is supplied from the stereo/SAP decoder IC404 to IC402 pins 12 (L-CH)/5 (R-CH). The line input audio (3-2 L/R) is cross-linked; when both jacks are used, the signals are supplied separately to the L and R channels, and when a plug is connected only to one jack, the connected signal is supplied to both channels. The L channel line is connected to IC402 pin 13 and the R channel line to pin 3.
IC402 selects the input using S2 and S3.
The specifications of IC402 are as follows.

(L-Channel)

Pin No.	Function
11	S3 control input. ("Hi" is applied to this pin when the tuning μP judges the Line (AUX) mode.) Hi: Pin 13 input – Pin 14 output Lo: Pin 12 input – Pin 14 output
12	S3 tuner audio input
13	S3 line-in audio input
14	S3 output

(R-Channel)

Pin No.	Function
11	S2 control input. ("Hi" is applied to this pin when the tuning μP judges the Line (AUX) mode.) Hi: Pin 3 input – Pin 4 output Lo: Pin 5 input – Pin 4 output
12	S2 tuner audio input
13	S2 line-in audio input
14	S2 output

The outputs at pins 14 and 4 of IC402 are supplied to IC403 pins 43 and 42 for the record/EE processing.

– ALC (IC403) –

(4-1 L/R)
The input at pins 43 (L-CH)/42 (R-CH) of IC403 are applied to record/palyback switches S5 (L-CH)/S1 (R-CH). S5 and S1 are controlled by the level at pin 17; Pin 17 goes "Lo" in modes other than playback. S5 and S1 selects the input at pins 43 and 42. The level fluctuations in the record signal input from pins 43 and 42 are detected by the ALC/LINE amplifier circuit to control the level so it is constant and the signal is output from pins 45 (L-CH)/40 (R-CH) via mute switches S6 (L-CH)/S2 (R-CH).
Line mute switches S6 and S2 are provided in the stage prior to pins 45 and 40. During loading pin 21 goes "Hi" and S6/S2 becomes open.

– fH Bias Trap (L404) –

(4-2 L/R)
This consists of lowpass filters in two stages and removes the 15.734 kHz horizontal sync signal leaking into the audio signal
- To prevent the Dolby NR from malfunctioning, and
- To remove the 70 kHz bias frequency to prevent buzz.

– Dolby NR (IC403) –

(4-3 L/R, 4-4 L/R)
The record signals input to iC403 via pins 46 (L-CH)/41 (R-CH) applied to the input amplifier. These signals are branched into the main signal (4-3 L/R) and EE signal (record monitor) (4-4 L/R). Monitor signal selection: S4 (L-CH)/S3 (R-CH)
IC403 Pin 17 Lo: EE signal
The EE signal is output from IC403 pins 44 (L-CH)/39 (R-CH). These are supplied to
- the RF converter
- audio output jack
- level meter

The main signal is applied to the adder (ADD) and the sub signal described later is added to it. The outputs at pins 12 (L-CH)/16 (R-CH) are signals with the only low-level high frequencies boosted. These signals are supplied to the record amplifiers (in IC403) via the record level controls (RT403 L/R). These signals are supplied to the audio head via the bias trap.

Sub Signal Route

Part of the E-E signal (sub signal) passing through S4 (L-CH)/S3 (R-CH) is supplied to the Dolby NR circuit.
The Dolby NR circuit extracts only the low-level high-frequency components from the sub-signal.
The Dolby NR circuit:
- Suppresses the sub-signal output when the input signal is high, so it is constant.
- Greatly compensates high frequencies with respect to high-level input signals without high-frequency components.
- Compensates the high frequencies slightly with respect to low-level input signals with many high-frequency components. In this case, hiss noise is not conspicuous due to the masking effect.

The sub-signal with only the low-level high frequency components is supplied to the adder to give it encoding (compression) characteristics.

– Record Level Control (RT403 L/R) –

(4-6 L/R)
In the Dolby NR system, the output level of the encoder and the input level of the decoder must always be equal. If they were not equal, the compression and expansion characteristics would be defective and the flatness of the frequency response would be degraded during recording and playback. To prevent this, RT403 L/R adjust the recording output of the Dolby NR circuit.

– Record Amplifier (IC403) –

(4-7 L/R)
The outputs at RT403 L/R are supplied via pins 11 (L-CH)/15 (R-CH) to the amplifiers in IC403. The record amplifiers are controlled by pin 24. Pin 24 go "Hi" during recording and output the amplified signals from pins 11 and 15. The

recording equalizers are connected to inside of IC403 and switch the frequency response in the SP, LP and EP modes.

- In SP the frequency response is determined by the SP EQ components connected to the circuits inside IC403.
- In LP the frequency response is determined by the SP EQ and LP EQ components connected in parallel.
- In EP the frequency response is determined by the SP EQ and EP EQ components connected in parallel.

The emphasis is applied from lower frequencies when the tape speed is slower.

– Record Mode Head Switching (IC401 L/R) –

(4-9 L/R)

The outputs (recording audio signals) at pins 3 (L-CH)/7 (R-CH) of IC403 on which the bias current generated at T401 is superimposed are supplied to the audio head. The audio head is controlled by IC401 L/R and is configured in the record mode.

During recording, "Hi" is applied to pins 5 of IC401 L/R to activate S2. Pins 7 are "Lo" and switches S1 turn off. These operations cause the head to be terminated with R401 L/R and the head is configured in the record mode.

The record current can be measured across TP401 L/R and TP402 L/R.

– Bias Trap (L402 L/R) –

(4-8 L/R)

A trap consisting of a parallel resonant circuit of L and C is inserted into the output of the record-amplifier to prevent the bias current from affecting the record-amplifier. This trap is resonated by the bias frequency and is set so its reactance becomes maximum.

– Bias Oscillator (T401) –

When a specified voltage is applied pin 4 of bias oscillator T401, the oscillation outputs are obtained at pins 1, 2 and 3. The full erase head is connected to pin 1, the audio erase head to pin 3 and the audio head to pin 2.

The level of the bias current following to the audio head can be adjusted by RT401 L/R.

"Hi" is applied to pin 4 in the record mode.

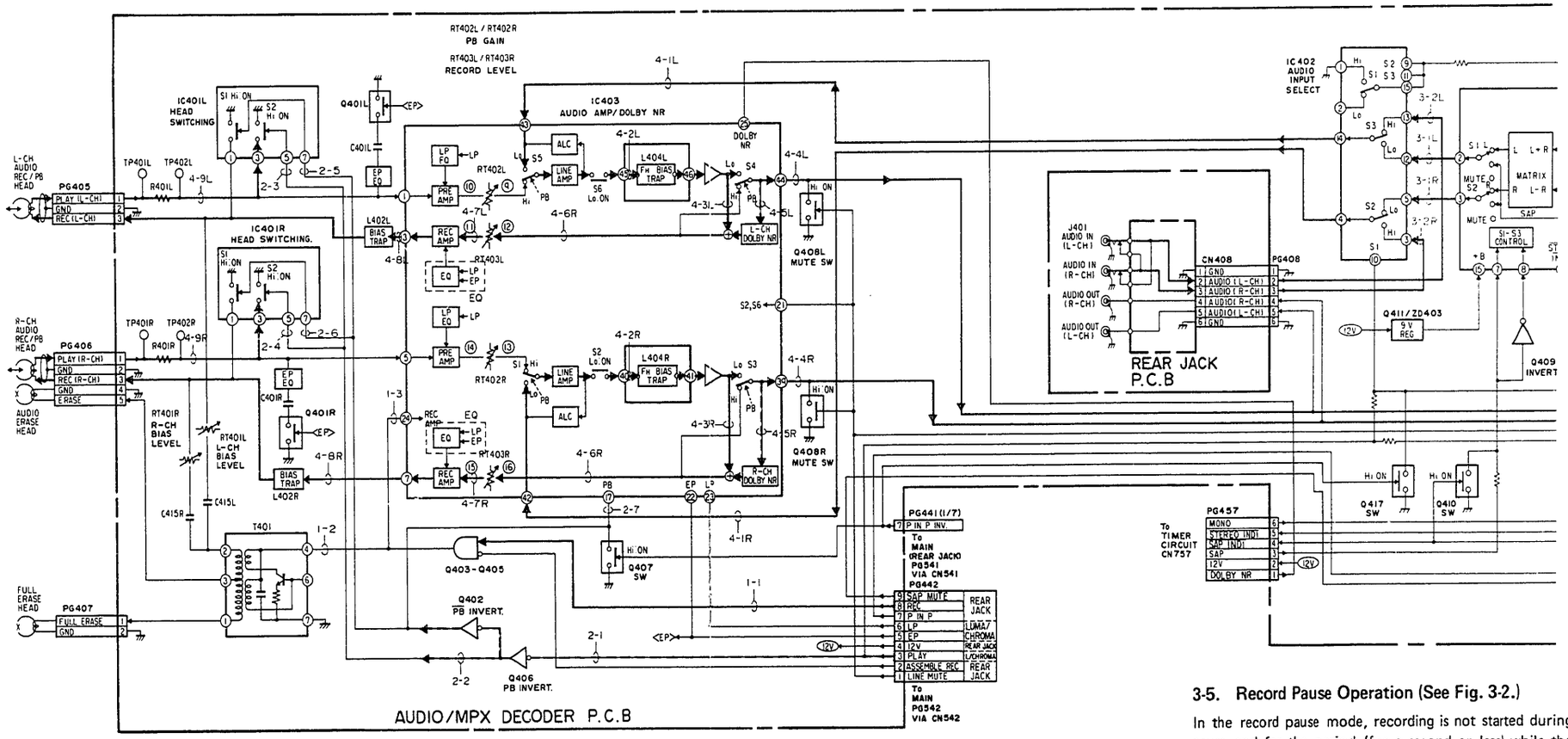


Fig. 3-2 EE/Record Operation

3-5. Record Pause Operation (See Fig. 3-2.)

In the record pause mode, recording is not started during pause and for the period (for a second or less) while the simplified assemble operation is performed after pause is released. This control is performed by the assemble record signal supplied from the system control μP. Immediately after pause is turned off, the ASSEMBLE REC: Hi signal is output by the assemble record control circuit in the servo circuit and the system control μP. This signal is applied to the gate circuits of Q403 – Q405 and makes the output of Q405 "Lo" to inhibit the operations by the record signal described previously.

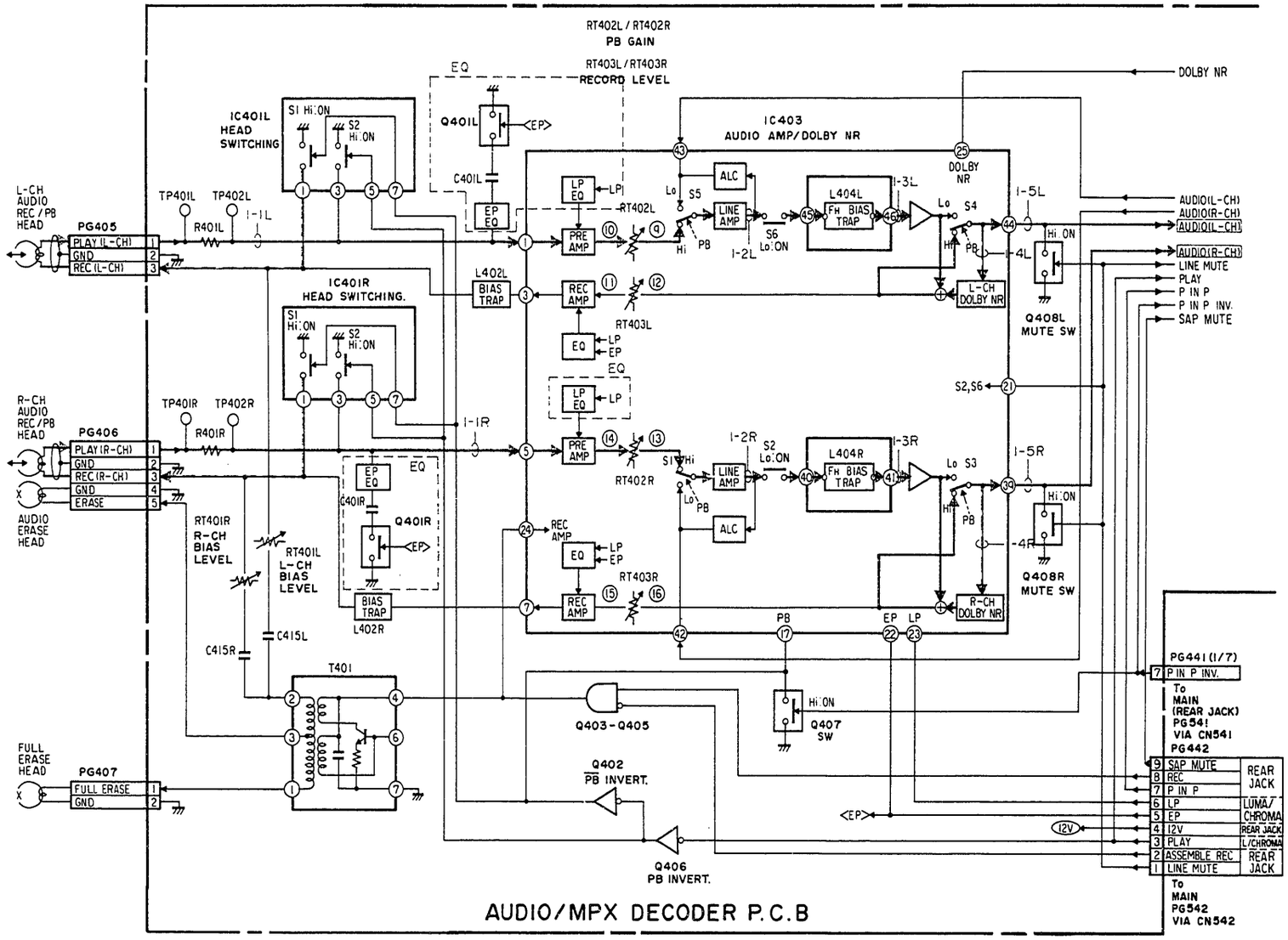


Fig. 3-3 Playback Operation

3-6. Playback Operation (See Fig. 3-3.)

The right and left channel head output signals are applied to preamplifier in the IC403. The output is then applied to the Dolby processing circuit where the Dolby noise reduction is performed. The output of the Dolby amplifier is then applied to the right and left channel outputs.

– Preamplifier (IC403) –

(1-1 L/R)
The audio signal from the head which is developed as a result of play switches S1 in IC401 L/R being turned "ON" is applied to preamplifier in the IC403. Preamplifiers are connected with RT401 L/R which adjust the feedback loop gain and regulate the playback output. The playback equalizer circuit (EP EQ: Q401 L/R and peripheral components, LP EQ: Inside of IC403) is provided in the input/output stages, and the characteristics in reverse to those during recording are applied to the playback audio output.

– Playback Muting (IC403) –

(1-2 L/R)
Playback muting switches S6 (L-CH)/S2 (R-CH) are provided in the output stage of line amp (IC403). It is operated by the MUTE signal and shuts off the audio output during trick play and playback loading.
The mute switch output is derived from pins 45 (L-CH)/40 (R-CH) and is supplied to the Dolby processing circuit to be decoded.

– Playback Dolby Processing –

(1-3 L/R to 1-5 L/R)
The audio signals applied to pins 46 (L-CH)/41 (R-CH) are then applied to a pair of amplifiers. (1-3 L/R)
The amplified signals are send to playback switches S4 (L-CH)/S3 (R-CH). S4 and S3 are activated during play and send the play signal to the Dolby NR circuit via the adder circuit. The Dolby decoder is composed of this loop. (1-4 L/R) The Dolby filtered audio is mixed with the incoming audio to reconstruct the audio signal to its original form before the record process with the exception that the inherent background noise from the video tape has been reduced. The outputs at pins 44 (L-CH)/39 (R-CH) are then applied to the line output jacks and are also mixed before being applied to the audio modulator in the RF converter. (1-5 L/R)

3-7. Audio Signal Selection – P IN P Mode (See Fig. 3-3.)

– P IN P INV. SW (Q407) –

When the P IN P INV. switch is pressed in the P IN P mode in which the played back picture appears on the main screen, the E-E picture appears on the main screen.
Q407 detects the P IN P INV. signal and forces pin 17 of IC403 to "Lo".
Switches S1 and S3 – S5 in IC403 select the E-E audio signal.

3-8. EE Signal Mute Control: IC402, IC404 (See Fig. 3-4.)

(1-1 to 1-5)
The audio input select IC (IC402) and MTS decoder IC (IC404) mute the EE audio signal leaked from the line input to the playback signal during playback.
The "PLAY" signal supplied via pin 9 to IC404 switches S1 and S2 in IC404. (1-1) This "PLAY" signal also goes through pin 10 to IC402. At pin 10 the "PLAY" signal (1-2) uses S1 in IC402 to place the control inputs of S2 and S3 on "Lo". (1-3) Thus, S2 and S3 select IC404 in the MUTE state. (1-4 L/R) This completely mutes audio signals from the line input.
In the P IN P mode, to prevent the muting of the audio signal input from the line when the main screen switches from a playback to EE picture, a "P IN P INV." signal applied to the base of Q417 grounds the collector. (1-5) This disables the "PLAY" signal usually supplied to IC402 and IC404.

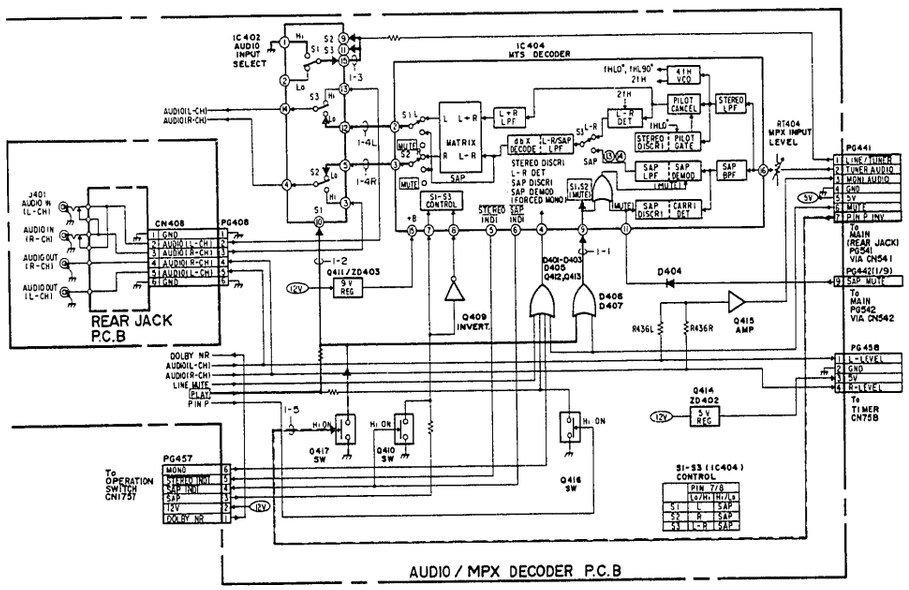


Fig. 3-4 EE Signal Mute Control

3-9. MTS Decoder (See Figs. 3-5 and 3-6.)

The tuner supplies the audio signal to the MTS decoder IC (IC404) via pin 16 after MPX Input Level control RT404 adjusts its level to the specified value. IC404 is a module IC which demodulates the MTS signal to a stereo signal or a second audio program (SAP) signal. IC404 has all filters necessary for demodulation.

– Stereo Lowpass Filter (50 kHz) –

Removes the SAP signal and telemetry signals.

– 4fH VCO (Voltage-Controlled Oscillator) –

Generates 2fH, 90°-phase fH and 0°-phase fH signals. The 2fH signal is used for L-R signal detection, the 90° fH signal for phase detection and the 0° fH signal for pilot cancellation.

– Pilot Gate –

Passes the pilot signal which has the same phase as the fH signal and detects the amplitude of the pilot signal to supply it to the pilot cancel and stereo discriminator circuits. When the output of the pilot gate exceeds the specified voltage, the stereo discriminator activates the stereo indicator driver.

– Pilot Canceller –

Uses the 0° fH signal to cancel the pilot signal.

– L+R Lowpass Filter (14 kHz) –

Removes the L-R signal and extracts the L+R signal.

– L-R Detector –

Uses the 2fH signal to demodulate the L-R signal.

– L-R/SAP Switch S3 –

Selects the L-R signal or SAP signal. Level at pin 8 controls signal selection.

– L-R/SAP Lowpass Filter (14 kHz) –

Eliminates high-frequency components.

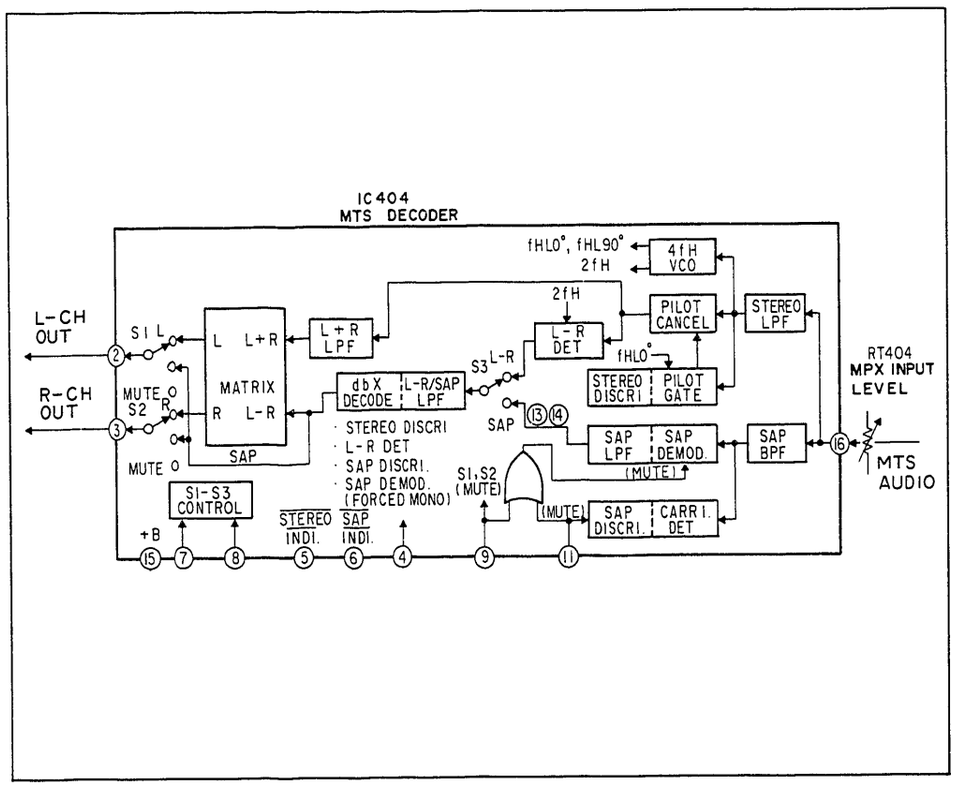


Fig. 3-5 MTS Decoder

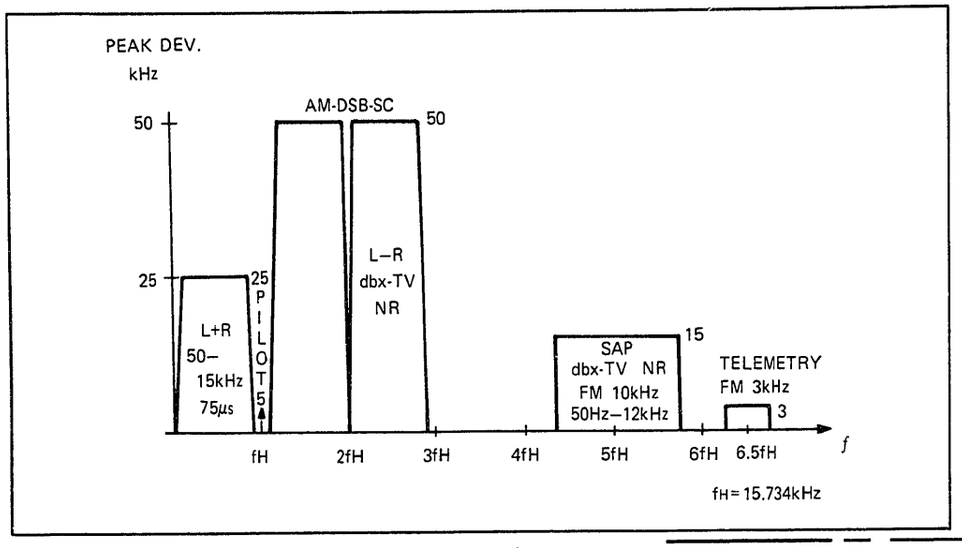


Fig. 3-6 Base Band Spectrum

– dbx Decoder –

Expands and deemphasizes the L-R/SAP signal which the broadcast station has compressed and preemphasized and retrieves the original audio signal.

– Matrix Circuit –

Produces the L and R signals from the L+R and L–R signals.

– Switches S1 and S2 –

Controlled by levels at pins 7, 8 and 9 to select L, R, L+R, SAP or MUTE signal.

– SAP Bandpass Filter –

Eliminates the L+R, L–R and telemetry signals and applies the SAP signal to the SAP demodulator and carrier detector.

– SAP Demodulator –

Demodulates the second audio signal in the base band.

– SAP Lowpass Filter –

Removes the FM components.

– Carrier Detector –

Detects the amplitude of the 5fH signal.

– SAP Discriminator –

Mutes the SAP signal when 5fH is not detected and also drives the SAP indicator.

3-10. MTS Decoder Control

Input select switch S1792 on the operation switch circuit board controls MTS decoder. The decoder operates as follows at each S1792 position (MONO, STEREO, SAP).

– S1792 : MONO Position (See Fig. 3-7) –

The "MONO" signal from PG457 pin 6 goes "Hi" and it is applied to pin 4. This signal stops the stereo discriminator, L-R detector, SAP discriminator and SAP demodulator. When the stereo and SAP discriminators stop, the stereo and SAP indicator output pins 5 and 6 become open (Hi). Stereo and SAP indicators do not light. Since the "SAP" signal at pin 3 of PG457 is open (Lo), the switch control input pin 7 goes "Lo" and pin 8 goes "Hi" via inverter Q409. S1 selects the L signal, S2 selects the R signal and S3 selects the L-R signal. The stereo and SAP circuits stop and only the L+R signal enters the matrix circuit. Therefore, a monaural signal (normal audio signal) is obtained at L/R outputs (pins 2 and 3) regardless of whether a stereo or SAP broadcast signal is received.

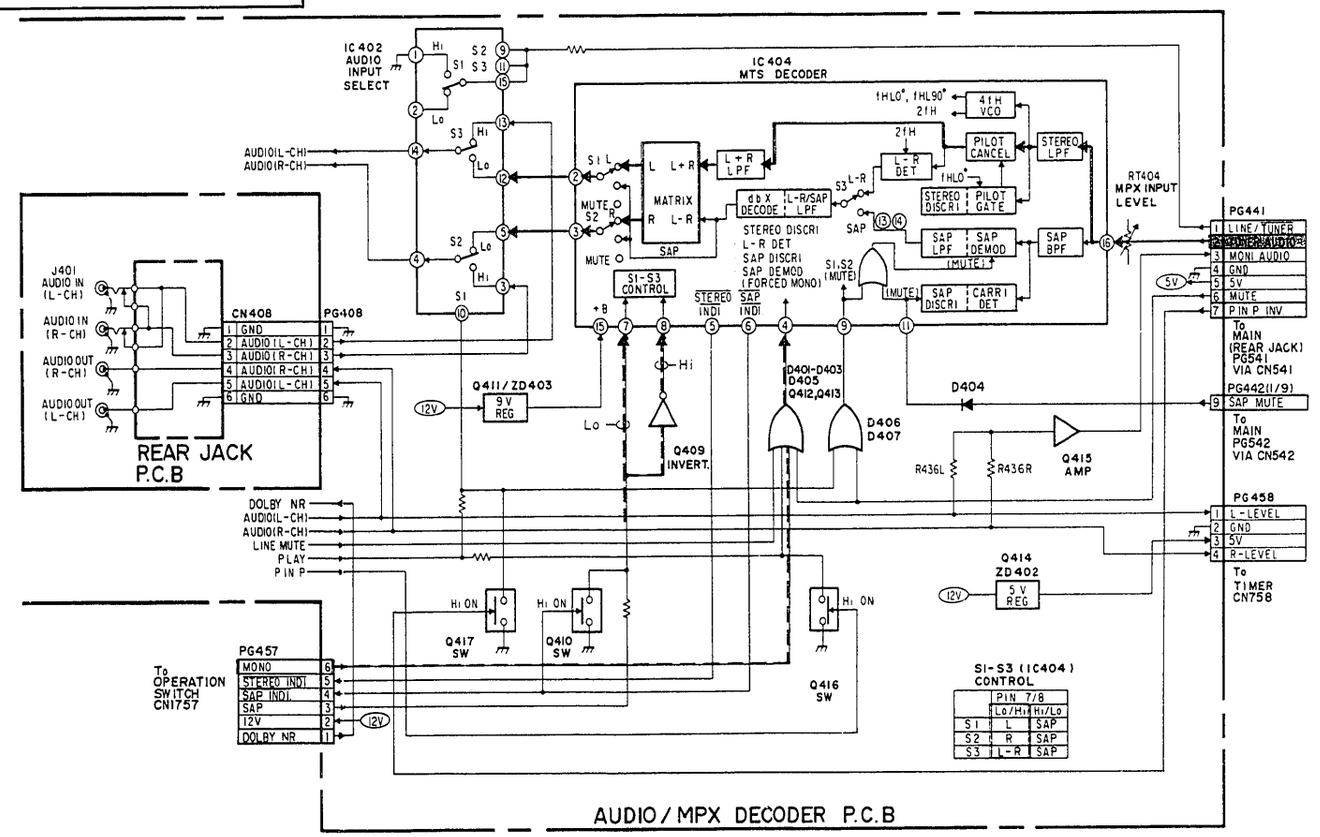


Fig. 3-7 MTS Decoder Control – S1792 : Mono Position

– S1792: STEREO Position (See Fig. 3-8.) –

- Normal broadcast reception:
  Because there is no pilot signal, the stereo discriminator opens (Hi) the stereo indicator output (pin 5). The SAP discriminator opens (Hi) SAP indicator output (pin 6) because there is no SAP carrier (5fH). Therefore, stereo and SAP indicators do not light. Switches S1 to S3 are controlled in the same way as in the monaural mode.
  Since only the L+R signal is input to the matrix circuit, a normal audio signal is obtained at L/R outputs (pins 2 and 3).
- Stereo broadcast reception:
  The stereo discriminator detects a pilot signal and places the stereo indicator output (pin 5) on "Lo" to light the stereo indicator.
  The L-R detector demodulates the L-R signal and applies it to S3.
  Because there is no SAP carrier (5fH), the SAP discriminator opens SAP indicator output (pin 5).
  Switches S1 to S3 are controlled in the same way as in the monaural mode.
  Since the L+R and L-R signals are input to the matrix circuit, a stereo signal is obtained at L/R outputs (pins 2 and 3).
- SAP broadcast reception:
  The SAP discriminator detects SAP carrier (5fH) and has the SAP indicator output (pin 6) "Lo" to light the SAP indicator. All other operations are the same as normal broadcast reception. A normal audio signal is obtained at L/R outputs (pins 2 and 3).
- Stereo/SAP simulcast reception:
  The SAP discriminator detects SAP carrier (5fH) and has the SAP indicator output (pin 6) "Lo" to light the SAP indicator. All other operations are the same as stereo broadcast reception. A stereo signal is obtained at L/R outputs (pins 2 and 3).

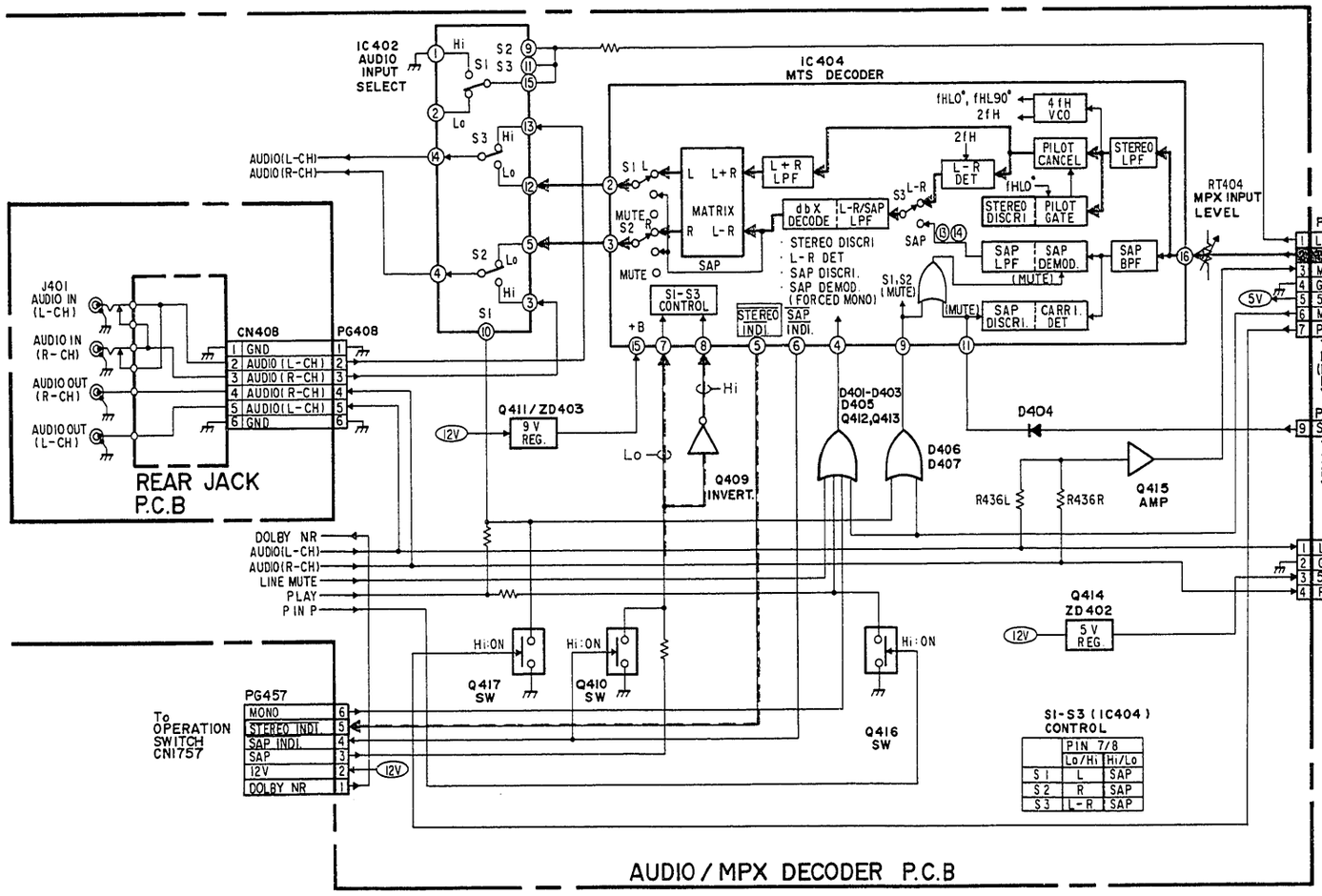


Fig. 3-8 MTS Decoder Control – S1792 : Stereo Position

– S1792: SAP Position (See Fig. 3-9.) –

- Normal broadcast reception:
  Because there is no pilot signal, the stereo discriminator opens (Hi) the stereo indicator output (pin 5). Because there is no SAP carrier (5fH), the SAP discriminator opens (Hi) the SAP indicator output (pin 6). Therefore, stereo and SAP indicators do not light.
  Since the "SAP" signal at pin 3 of PG457 normally goes "Hi" when S1792 is in SAP position, switch control input pin 7 goes "Hi" and pin 8 goes "Lo" via inverter Q409. Switches S1 to S3 select a SAP signal. However, as the SAP indicator output is open in modes other than SAP broadcast reception, the voltage at the cathode of SAP indicator D755 in the timer circuit grounds the collector of Q410 via PG457 pin 4. Therefore, switch control input pin 7 goes "Lo" and pin 8 goes "Hi" via inverter Q409. S1 selects the L signal, S2 the R signal and S3 the L-R signal. Since only the L+R signal inputs to the matrix circuit, a normal audio signal is obtained at L/R outputs (pins 2 and 3).
- Stereo broadcast reception:
  The stereo discriminator detects the pilot signal and causes the stereo indicator output (pin 5) "Lo" to light the stereo indicator. All other operations are the same as in normal broadcast reception.
  A normal audio signal is obtained at L/R outputs (pins 2 and 3).
- SAP broadcast reception:
  Since there is no pilot signal, the stereo discriminator opens (Hi) stereo indicator output (pin 5). The SAP discriminator detects the SAP carrier (5fH) which causes the SAP indicator output (pin 6) to go "Lo" and light the SAP indicator.
  The SAP demodulator demodulates the SAP signal and applies it to S3 via the SAP LPF, pin 14 and pin 13.
  The "SAP" signal output from PG457 pin 3 goes "Hi" and the switch control input pin 7 goes "Hi" and pin 8 goes "Lo" via inverter Q409. Switches S1 to S3 select the SAP signal.
  A SAP audio signal is obtained at L/R outputs (pins 2 and 3).
- Stereo/SAP simulcast reception:
  The stereo discriminator detects the pilot signal and causes the stereo indicator output (pin 5) "Lo" to light the stereo indicator, but other operations are the same as in the SAP broadcast reception.
  A SAP audio signal is obtained at L/R outputs (pins 2 and 3).

– P IN P Mode –

During tape playback, the "PLAY" signal is applied to pin 4 to disable the stereo and SAP indicator outputs.
To enable indicator outputs in the P IN P mode, the "P IN P" signal is applied to the base of Q416 to ground the collector. The "PLAY" signal is disabled.

– Mute Control –

Tuning μP IC801 in the F. S tuning circuit outputs the:
- "LINE" signal when line input is selected.
- "MUTE" signal when the ERASE button is pressed in the channel select mode.

These signals go to pins 4 and 9 via PG441 pin 6. The signal at pin 9 switches S1 and S2 to MUTE. The signal at pin 4 disables the stereo and SAP indicator outputs.
The IC in the IF circuit outputs the "SAP MUTE" signal if the SAP carrier is weak in an area where field strength is low. This "SAP MUTE" signal is applied to pin 11 via PG442 pin 9.
The signal at pin 11 disables the SAP demodulator and SAP discriminator. The MTS decoder selects a normal or stereo broadcast.

– Indicator Output Disable –

When power is turned on/off, the system control μP, IC901, outputs the "LINE MUTE" signal to mute the audio signal at the audio circuit output stage. (Q408 L/R) Meanwhile, the "LINE MUTE" signal is applied to pin 4 to disable the stereo and SAP indicator outputs.

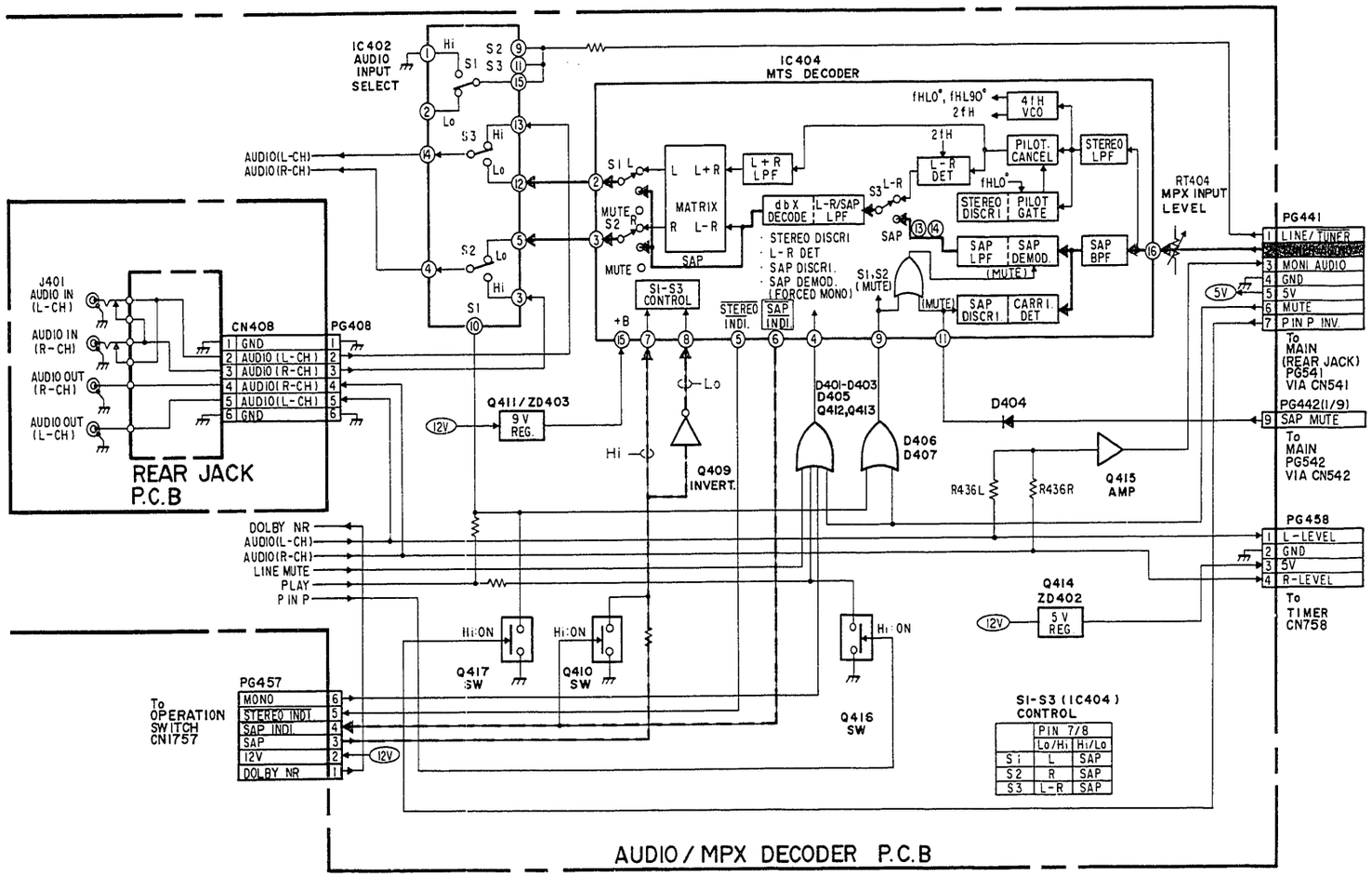


Fig. 3-9 MTS Decoder Control – S1792 : SAP Position

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